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INFRARED RESPONSE OF IMPURITY DOPED SILICON MOSFET'S (IRFET'S)

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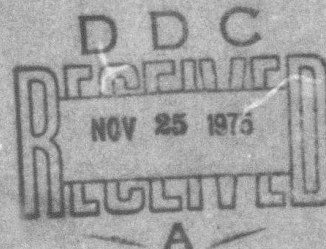Approved for Public Release; Distribution Unlimited

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Operation and characteristics of the indium doped infrared sensing MOSFET (IRFET) are described. Responsivities of over 40 milliwatts/microjoule have been observed with only small channel width to length ratios and large area devices. Much higher responsivities would be possible with smaller

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area devices and larger width to length ratios. This device is anticipated to be particularily usefull in the 3 to 5 micrometer wavelength range, and operates at temperatures less than 50°K.

Preliminary results have been obtained on the operation of the gallium doped infrared sensing MOSFET at 24.5 ^{o}K.

A theoretical analysis shows that all surface type semiconductor infrared detectors, CID, CCD, or IRFET have essentially the same maximum attainable signal to noise ratio under shot noise or background limited operation. Noise measurements on the IRFET show that shot noise or background limited operation can be acheived for integration periods of less than ten seconds in non-optimized device structures.

These results suggest that the infrared sensing MOSFET or IRFET might indeed be most usefull in infrared imaging applications in the near, middle, and far infrared.

TECHNICAL REPORT SUMMARY

Operation of the indium doped infrared sensing MOSFET (IRFET) has been demonstrated. An examination of the device operation shows that the results developed previously for the gold doped devices can be readily extended to the indium doped devices.

Indium doped devices are anticipated to be particularly useful in the 3 to 5 micrometer wavelength range since their response peaks in this range.

A process has been developed for the diffusion of gallium from doped oxide sources into boron doped wafers. An investigation of the MOS capacitor C-V characteristics indicates that convenient gallium concentrations can be achieved by this technique. This process is directly applicable to the MOSFET device and double doped, gallium and boron doped, infrared sensing MOSFETs produced by this technique. Preliminary results on these latter devices at low temperatures are most encouraging.

An investigation has been made of noise mechanisms. It has been shown that theoretically all surface type solid-state devices have essentially the same maximum attainable signal to noise ratio, these include CCD's, CID's, and IRFET's. It has been found that shot noise or background limited operation of the IRFET can be achieved for integration periods of less than ten seconds.

Based on these observations we feel that, for the most part, operation of the IRFET over the entire infrared region, near, middle, and far should be relatively easily achieved. Shot noise or background limited operation should also be achieved over a wide range of operating conditions.

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THE INFRARED SENSING MOSFET (IRFET)

GOLD-DOPED DEVICES

A detailed treatment of the characteristics of these devices has been given in:

(I) AFCRL-TR-75-0168 semiannual technical report for the period 1 Aug. 1974 - 31 Jan. 1975.

(II) "Experimental Characterization of Gold-Doped, Infrared-Sensing MOSFET," by W. C. Parker and L. Forbes, to be published in IEEE Transactions on Electron Devices, and scheduled to appear October 1975.

This page is included primarily for completeness, if necessary additional copies of either of these items may be obtained. Copies of item (I) may be obtained by qualified requestors from the Defense Documentation Center, all others should apply to the National Technical Information Service. Copies of item (II) may be obtained from the co-author, L. Forbes. In addition, the results were presented in part as paper 4.8 at the International Electron Device Meeting, Washington, D. C., 1974.

INDIUM DOPED DEVICES

EXPERIMENTAL VERIFICATION OF OPERATION OF THE [**]
INDIUM DOPED INFRARED SENSING MOSFET

The infrared sensing MOSFET was originally proposed [1] as an extrinsic silicon detector which might be most useful in infrared imaging and target tracking applications. Since that time operation of gold doped devices, employing response from both the gold donor and acceptor levels, has been investigated and described in detail [2,3]. The gold doped detectors, however are limited to the near infrared portion of the spectrum or wavelengths less than 3.0 micrometers. In this short report we provide experimental verification of operation of the indium doped extrinsic silicon detector whose infrared response extends out to 8.0 micrometers and which peaks in the often employed 3.0 to 5.0 micrometer wavelength range.

The infrared sensing MOSFET (IRFET) employs photoionization of impurity centers in the surface depletion or space charge region behind the strongly inverted surface channel as the infrared detection mechanism. Photoionization of these centers modulates the space charge in this depletion region and modulates the threshold voltage and conductivity of the MOSFET [1]. In the case of indium doped devices, the indium centers are first filled with holes by accumulating the surface, the transistor is then turned on by applying a large positive gate voltage. If the indium centers in the surface depletion region subsequently change charge state by emission of holes to the valence band the conductivity between the source and drain of the device will decrease due to the increase in negative space charge associated with ionized indium centers in the surface depletion region. Theoretically then, there are two distinctly different limiting conductivity states, one corresponding to the case where the indium centers are filled with holes, or in the neutral charge


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state, and one corresponding to the case where the indium centers are ionized or in the negative charge state.

To verify operation of this new detector for the middle infrared region we have fabricated n-channel MOSFET's using a 4000A gate oxide on 3 to 5 ohm-cm indium doped silicon wafers obtained from General Diode Corporation, Framingham, Massachusetts. These were only single indium doped wafers and not double indium and boron doped as specified in the original design [1]. The double doping is in fact more desireable in order to provide for a fast and reproducible reset operation during surface accumulation, the boron doping would assure the presence of appreciable number of holes for the indium centers to capture, but is not necessary to unequivocally demonstrate operation of the device. Fig. 1 shows the two limiting cases for conductivity of the indium doped IRFET, in Fig. 1(a) the indium centers have been arranged to be in the neutral charge state by first accumulating the surface and then measuring the transistor characteristics. The measurements have been made at 47°K to avoid allowing the indium centers to thermally emit holes to the valence band. In Fig. 1(b), the indium centers have been allowed to emit holes to the valence band, or become ionized, and then the temperature lowered to 47°K. Large changes in conductivity of the IRFET have been observed with the change in charge state of the indium impurity centers in the surface space charge or depletion region.

When operating this type of device as an infrared detector the temperature must be low enough to avoid thermal ionization of the indium centers due to thermal emission. The thermal emission rate for holes from indium centers in silicon has been determined by measuring the time constant of the decay between the two limiting conductivity states as a function of temperature. Fig. 2 shows these results where the time constant, τ, is the reciprocal of of the thermal emission rate, e_p, and yields a thermal ionization energy,

INDIUM DOPED MOSFET

(A)

I_{DS}
200
$\mu A/DIV$
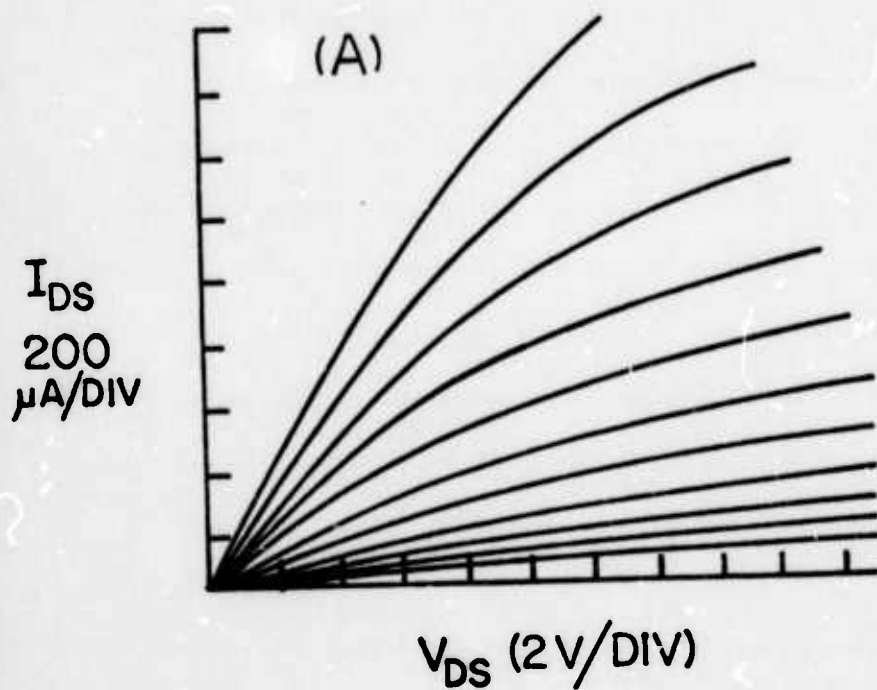
INDIUM CENTERS
NEUTRAL

(SURFACE ACCUMULATED
PRIOR TO CURVES)

V_{GS}
2V/STEP

V_{DS} (2V/DIV)

V_{BG} = -2.5 V
47°K

(B)

I_{DS}
200
$\mu A/DIV$
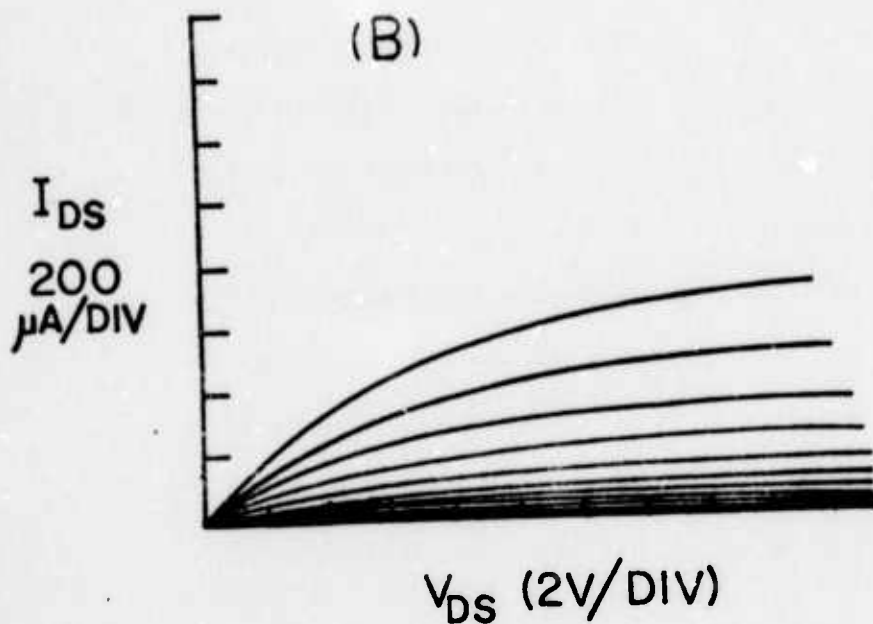
INDIUM CENTERS
IONIZED
(NEGATIVE)

V_{GS}
2V/STEP

V_{DS} (2V/DIV)

V_{BG} = -2.5 V
47°K

Figure 1. Indium Doped MOSFET Characteristics for the Two Limiting
Indium Charge States

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after including the factor $T^{-3/2}$ [4], of 0.167 eV. To the best of the authors' knowledge, the thermal emission rate of the indium center in silicon has not previously been determined. Also shown in Fig. 2 are the previously determined thermal emission rate for holes from gold donor centers [4,2,3] and the estimated characteristics for gallium centers. Basically longer wavelength detectors mean shallower level impurities and lower temperatures of operation.

Measurements have also been made of the infrared response of these detectors at 40°K by illuminating the IRFET with monochromatic radiation and determining the time constant associated with the decay in conductivity, as well as investigating the more detailed device characteristics. These results have been found to correspond to the previous design criteria and will be reported on in more detail in the next section.

In conclusion, the results presented here, we feel, adequately demonstrate operation of the indium doped silicon IRFET, and provide verification that the previous results on gold doped devices [2,3] can be extended by use of shallower level impurities as indium.
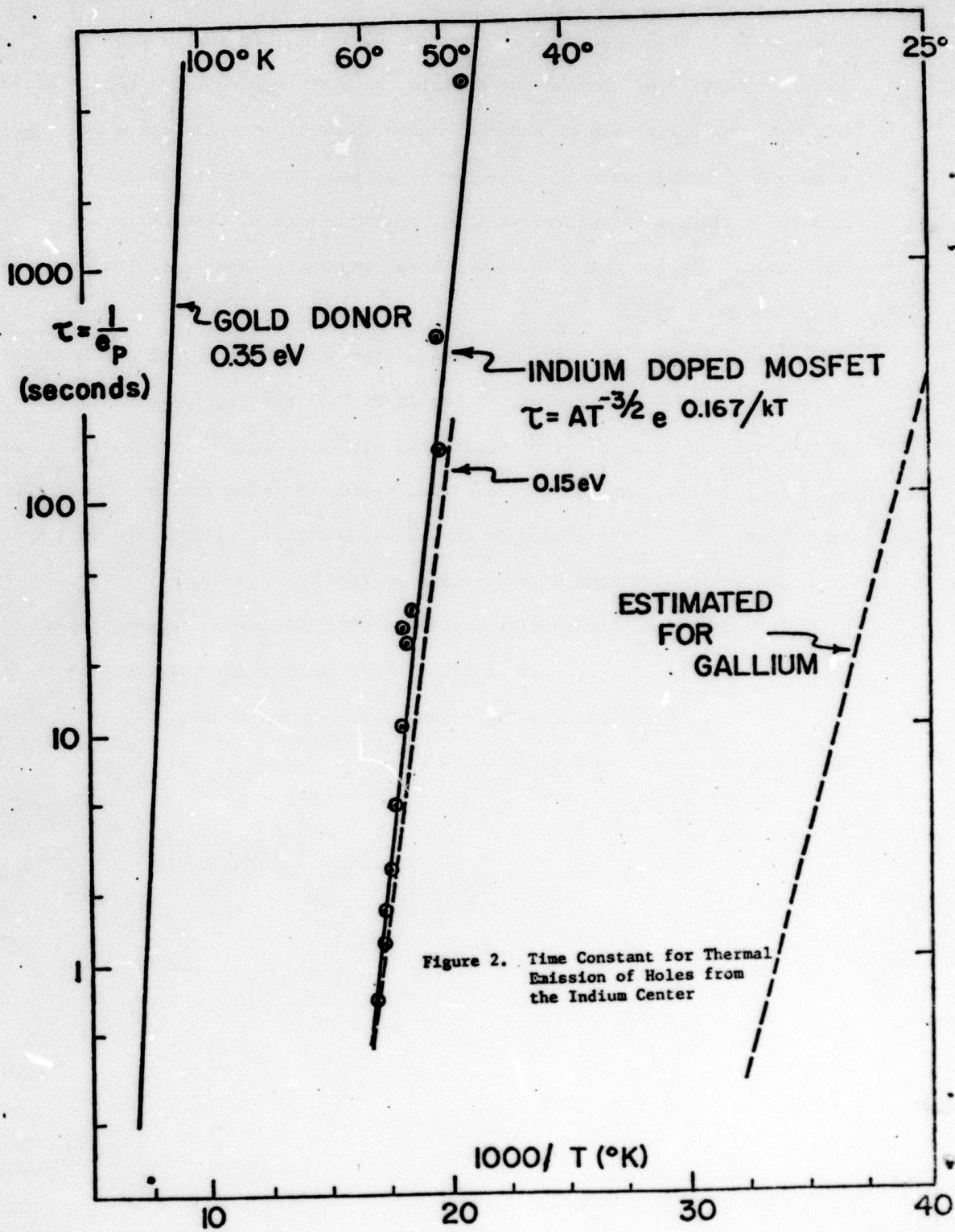
Figure 2. Time Constant for Thermal Emission of Holes from the Indium Center

1. L. Forbes and J. R. Yeargan, "Design for Silicon Infrared Sensing MOSFET," IEEE Trans. on Electron Devices, Vol. ED-21, pp. 459-462, Aug. 1974.

2. W. C. Parker, L. L. Wittmer, J. R. Yeargan and L. Forbes, "Experimental Characterization of the Infrared Response of Gold-Doped Silicon MOSFETs (IRFETs)," presented as paper 48 at International Electron Device Meeting, Washington, D. C., Dec. 1974.

3. W. C. Parker and L. Forbes, "Experimental Characterization of Gold Doped Infrared Sensing MOSFET," IEEE Trans. on Electron Devices, to be published.

4. C. T. Sah, L. Forbes, L. L. Rosier, A. F. Tasch, and A. B. Tole, "Thermal Emission Rates of Carriers at Gold Centers in Silicon," Appl. Phys. Lett., Vol. 15, pp. 145-148, 1969.

CHARACTERISTICS OF INDIUM DOPED INFRARED SENSING MOSFET

INTRODUCTION

Interest in infrared detectors that operate in the 3.0 to 5.0 micron wavelength range stems primarily from the fact that an atmospheric window exists in this region which allows transmission with very little attenuation. The spectral radiance of a $300^{\circ}K$ blackbody source also begins to peak in this region [4]. The basic objective of this report is to present experimenatlly determined data concerning the infrared sensing characteristics of the indium center in the surface space-charge region of a metal-oxide-silicon field-effect transistor (MOSFET). This data is then utilized to determine if our mathematical model of the IRFET is valid.

As seen from Figure 1, indium introduces an acceptor level within the bandgap of silicon [5]. The indium center can be ionized through the emission of holes to the valence band of silicon. Any sufficient thermal or optical excitation will result in the ionization of the indium center as depicted in the figure.

The design and fabrication of the indium-doped MOSFETs has been performed in the University of Arkansas Solid-State Device Laboratory. Their theoretical operation was then challenged by comparison with experimentally determined operating conditions.

THEORETICAL OPERATION

The IRFET, which is operated at low temperatures, employs impurity photo-ionization to modulate its source to drain conductance. The p-type substrate is doped with indium and a shallow level acceptor, boron. The temperature of operation, less than $45^{\circ}K$, is chosen such that the boron will be fully ionized and the indium will have a decay time constant in the thousands of seconds range [6]. This essentially eliminates the thermal emission rate, e_p^t, and in-
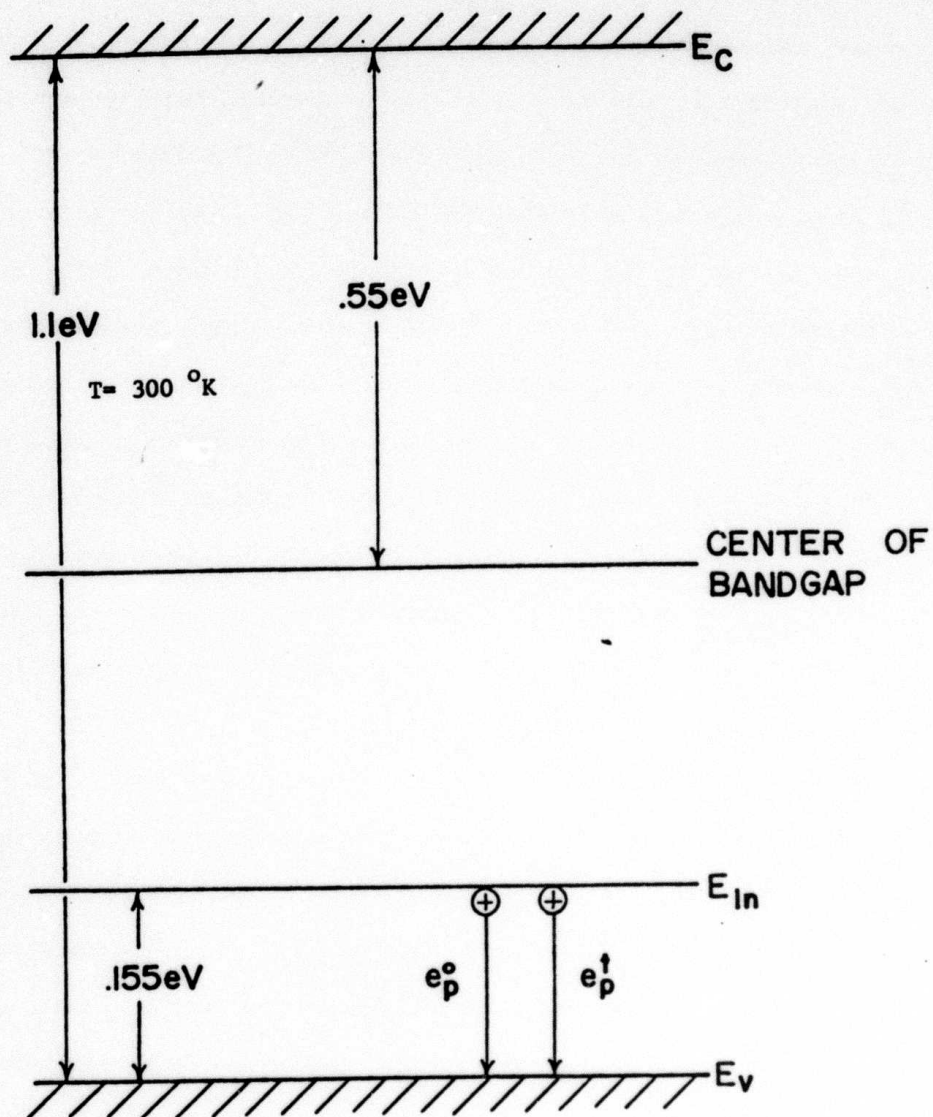
Figure 1   The Indium Acceptor Level In Silicon

sures that the ionization of the indium centers will be induced by incident infrared radiation (photoionization).

A cross section of the indium doped MOSFET is shown in Figure 2. This device is preset by the application of an accumulation voltage to the gate electrode. This corresponds to a negative voltage for an n-channel MOSFET. This enables the indium centers in the surface space charge region to return to their neutral charge state through the capture of a hole.

If infrared radiation in the 1.0 to 8.0 micron wavelength range now illuminates the device, the indium center will be photoionized by the emission of a hole to the valence band. The photoionization changes the net space charge from a net neutral to a net negative quantity. This change in charge state modulates the conductance of the surface inversion channel between source and drain since the conductance is a function of the number of ionized impurity centers in the space charge region. This process is also shown in Figure 2. There is no way that the indium centers can again become neutral unless an accumulation voltage is applied, since there are no free carriers present in the depletion region of the MOSFET.

Three processes can take place between the valance band of silicon and the indium impurity center [7]. The capture process, c_p, allows the indium center to capture a hole from the valence band. This process occurs only during the reset of the device. The thermal emission, e_p^t, is the rate at which the indium centers are ionized due to available thermal energy. The optical emission, e_p^o, is the rate at which the indium centers can be photoionized by incident infrared radiation. Due to the temperature dependence of the thermal emission rate, it becomes negilible with respect to the optical emission rate at the temperature of operation. Therefore, since the time constant of the indium ionization is related to the reciprocal of the emission rate of holes
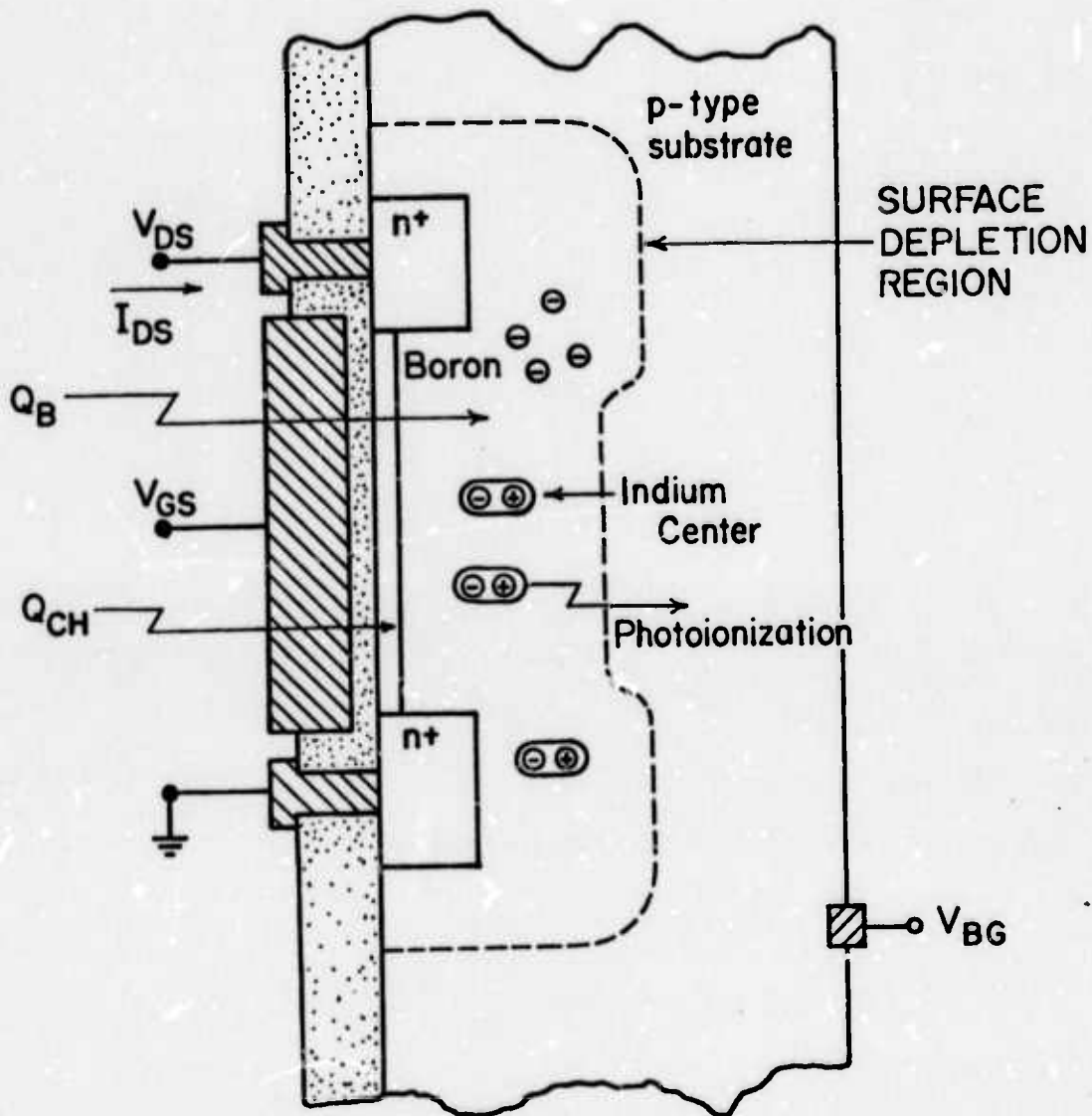
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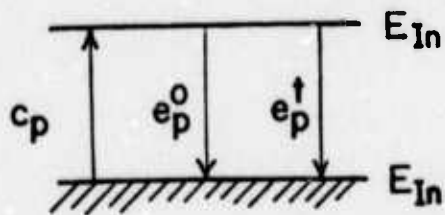
Figure 2   Cross-Sectional View of the Indium-Doped MOSFET

to the valence band, the time constant, τ, becomes

$$\tau = 1/e_p^o .$$
(1)

DEVELOPMENT OF DEVICE EQUATIONS

If the IRFET has been preset at low temperatures, the effective doping of the p-type substrate, N_I, is simply the boron concentration, N_A, since the indium centers are not ionized (neutral charge state). However, when photons of the appropriate energy are incident upon the device, the effective doping becomes $N_A + N_{In}$ due to the photoionization of the indium centers. In order to reset the device, an accumulation voltage is again applied.

This change in effective doping between the two distinct charge states of the indium center (neutral and negative) has a direct effect upon the threshold voltage of the device. The threshold voltage for an n-channel device can be written as

$$V_T = V_{FB} + 2\emptyset_f + Q_B/C_o,$$
(2)

where V_{FB} is the gate voltage required to establish the flat-band condition, $\emptyset_f$ is the Fermi potential, C_o is the gate oxide capacitance per unit area, and Q_B is the charge in the surface depletion layer generated by the impurity dopants [8]. It is through Q_B that the effective doping effects V_T. The expression for Q_B is;

$$Q_B = (2\kappa_{Si}\epsilon_o q\ N_I(2\phi_f - V_{BG}))^{\frac{1}{2}} ,$$
(3)

where κ_{Si} is the relative dielectric constant of silicon, ϵ_o is the electrical permittivity of free space, q is the electronic charge, and V_{BG} is a reverse-bias substrate voltage which tends to ionize additional impurity dopants in the space-charge region of the MOSFET [8].

If the IRFET is held at a constant operating temperature and the constants of equations 2 and 3 are collected, the threshold voltage may be rewritten as

$$V_T = A + B \sqrt{N_I} \quad , \tag{4}$$

where $A = V_{FB} + 2\phi_f$ and $B = (2\kappa_{Si}\epsilon_o q(2\phi_f - V_{BG}))^{\frac{1}{2}}/C_o$. The Fermi potential and the positive surface charge density, Q_{SS}, which is process dependent are assumed to be constants. Indeed, the Fermi potential is itself a function of the effective doping, but may be considered constant without appreciable error because of the greater magnitude of other terms in the equation, primarily V_{BG}.

It is evident from equation 4, that when the indium centers are ionized the threshold voltage of the device will increase. Defining the indium ionized as a final condition and the indium neutral as an initial condition, the change in threshold voltage between the two charge states, ΔV_T, can be expressed as

$$\Delta V_T = V_T^f - V_T^i = B \ (\sqrt{N_A + N_{IN}} - \sqrt{N_A}) \ . \tag{5}$$

This may be further reduced to

$$\Delta V_T = B\sqrt{N_A} \ (\sqrt{1 + N_{In}/N_A} - 1 \ ), \tag{6}$$

by factoring out common terms.

When illuminated with infrared radiation, the indium centers become negative with respect to time according to

$$N_T(t) = N_{In} \ (\ 1 - \exp(t/\tau) \ ) \tag{7}$$

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where $N_T(t)$ is the number of ionized indium centers as a function of time and τ is the time constant defined by equation 1 [7]. An expression for the time dependence of the threshold voltage can be derived by combining equations 6 and 7. The resulting equation becomes

$$V_T^L(t) = V_T^i + \Delta V_T(t)$$

$$= V_T^i + B\sqrt{N_A}(\sqrt{1 + N_{In}(1 - \exp(-t/\tau)/N_A} - 1) \qquad (8)$$

where $V_T^L(t)$ is the threshold voltage as a function of illumination time.

The two basic operating regions of the MOSFET are the linear and saturation regions. Equations relating drain current to drain voltage are well known and are found in most solid-state handbooks [5, 8]. In the linear region of operation, $V_{GS} - V_T > V_{DS}$, the device equation becomes

$$I_{DS} = \frac{\mu C_o W}{2L} (2V_{DS} (V_{GS} - V_T) - V_{DS}^2) \quad , \qquad (9)$$

where I_{DS} is the drain-to-source current, μ is the surface carrier mobility, W/L is the channel width to length ratio, V_{DS} is the drain to source voltage, and V_{GS} is the applied gate voltage.

In the saturation region of operation, $V_{GS} > V_T$ and $V_{GS} - V_T < V_{DS}$, the MOSFET equation becomes

$$I_{DS} = \frac{\mu C_o W}{2L} (V_{GS} - V_T)^2 . \qquad (10)$$

In both equations, 9 and 10, the gate oxide capacitance per unit area, C_o, may be calculated according to

$$C_o = \kappa_{ox}\epsilon_o/t_{ox}, \qquad (11)$$

where κ_{ox} is the dielectric constant of SiO_2 and t_{ox} is the thickness of the gate oxide.

An observation of equations 9 and 10 reveals that I_{DS} will decrease as the magnitude of V_T increases. Therefore, by defining the final and initial states as before, an expression for the photocurrent, ΔI_{DS}, may be derived. For the linear region this becomes

$$\Delta I_{DS} = \frac{-\mu C_o W}{L} (\Delta V_T) V_{DS}, \tag{12}$$

and in the saturation region;

$$\Delta I_{DS} = \frac{-\mu C_o W}{L} (\Delta V_T) (V_{GS} - V_T - \Delta V_T/2). \tag{13}$$

The negative sign in the above two equations indicates that the drain to source current decreases after illumination. This result is intuitively reasonable since the threshold voltage increases during ionization and the threshold voltage of a depletion mode device is defined as the applied gate voltage where drain to source conduction is terminated.

Expressions describing the photocurrent as a function of time may be derived by substituting equation 8 into equations 12 and 13. Equation 12 then becomes

$$I_{DS}^L(t) = \frac{-\mu C_o W}{L} V_{DS}(V_{GS} - V_T^i - B\sqrt{N_A}(\sqrt{1 + \frac{N_{In}(1-\exp(-t/\tau)}{N_A}} - 1) - V_{DS}/2, \tag{14}$$

and equation 13 becomes

$$I_{DS}^L(t) = \frac{-\mu C_o W}{2L} (V_{GS} - V_T^i - B\sqrt{N_A}(\sqrt{1 + \frac{N_{In}(1-\exp(-t/\tau))}{N_A}} - 1))^2, \tag{15}$$

where $I_{DS}^L(t)$ is the drain to source current as a function of illumination time. Equations 14 and 15 are valid only if the indium centers are in their neutral charge state at $t = 0$.

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MEASUREMENT TECHNIQUE

The IRFET was mounted in the sample holder of a model AC-2-110, open-cycle, cryo-tip* refrigerator manufactured by Air Products and Chemicals, Inc. The IRFET was completely sealed in this holder except for a 1/8 inch aperature covered with a piece of 1.5 mm fused-quartz directly in front of it. This was necessary in order to block out most of the incident background radiation which eminated from the $300^\circ K$ cryo-tip* shroud. A silicon window covering one port in the shroud, in conjunction with a germanuim filter, served to eliminate any extraneous light and to suppress the higher order modes of diffracted light. A diagram of the mounted IRFET is shown in Figure 3. The monochromatic light source consisted of a Bausch and Lomb high-intensity grating monochromator. The tungsten filament light source of this monochromator was employed out to wavelengths of 2.5 microns. At this point, a Carborundum gas igniter, model E-2055-1, which approximates a $1600^\circ K$ black-body, was employed as the light source. The change in sources was made since the relative output flux of the Carborundum gas igniter is greater than that of the tungsten filament for wavelengths longer than 2.5 microns.

The temperature of the IRFET was determined by monitoring the resistance of a model 1716 cryogenic platinum resistance temperature sensor, obtained from Weed Instrument Co., Inc. Eleven calibration points were furnished with the resistor ranging in temperature from $4^\circ K$ to $373^\circ K$. An IBM subroutine was then employed in order to relate the temperature to the resistance through an eighth-order polynomial so that an accurate determination of intermediate values of temperature could be made.

All voltages were measured with Fluke Digital Multimeters 8000A, as was the resistance of the temperature sensor. The current measurements were performed by monitoring the voltages across a precision resistor with a Keithley
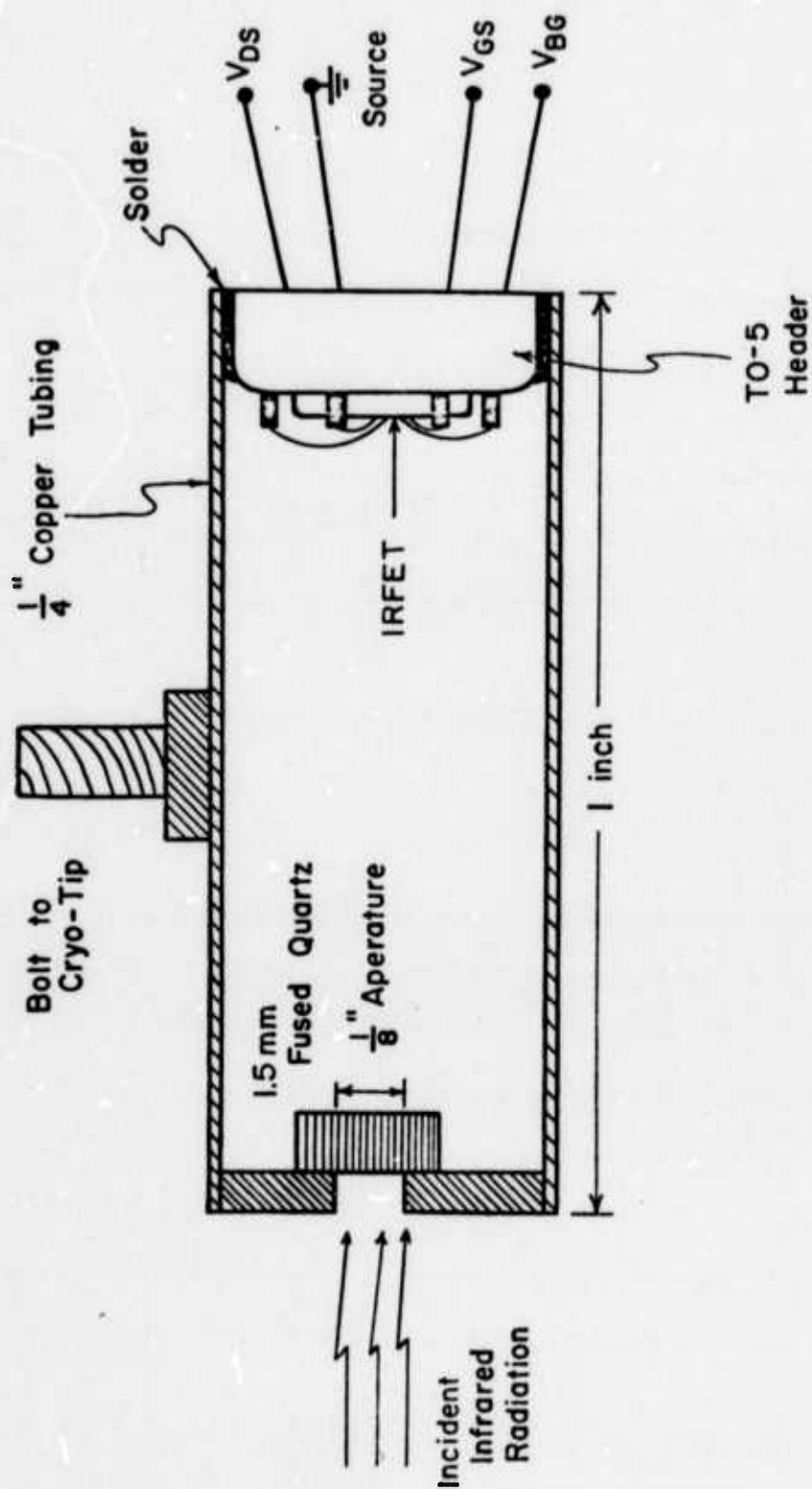
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*Trademark of Air Products and Chemicals Inc.

Figure 3 Cross-Sectional View of the IRFET Mounted in the Sample Holder

Electrometer 602 and recording their values on a Hewlett Packard 7035B X-Y
Recorder. This method of current measurement was employed so that loading upon
the IRFET would be minimal. A flow chart of the measurement technique is shown
in Figure 4.

DEVICE FABRICATION

The n-channel MOSFETs were fabricated on double-doped silicon wafers
(indium and boron doped) with a 100 orientation. Due to the difficulties en-
countered in obtaining an induim diffusion source and in the diffusion process
itself [9], we obtained a special order of silicon wafers that had been grown
with both the indium and boron impurities added. The wafers were obtained from
General Diode Corporation, Framingham, Mass. Our specifications were that the
wafers contain the following concentrations: $N_A = 1 \times 10^{16}/cm^3$, $N_{In} = 4 \times 10^{15}/cm^3$,
and less than $5 \times 10^{14}/cm^3$ residual impurities. However, after extensive measure-
ments were made on the MOSFETs and MOS capacitors we were forced to conclude
that the wafers used for IRFET fabrication contained $N_{In} = 10^{16}/cm^3$ and $N_A = 10^{13}/cm^3$.
This was very unfortunate since the substrate resistivity of the IRFET becomes
quite high at low temperatures due to the low concentration of boron present.
At this time, wafers meeting our specifications have not yet been obtained.

Standard silicon technology was employed to fabricate the MOSFET. The
n+ source and drain regions were formed by a phosphorous diffusion. The gate
oxides of our experimental devices are $5400^\circ A$ thick and the channels have a width
to length ratio of 8.17 in a circular geometry. The oxide thickness was veri-
fied by measuring the gate capacitance on a Boonton Capacitance Meter, Model
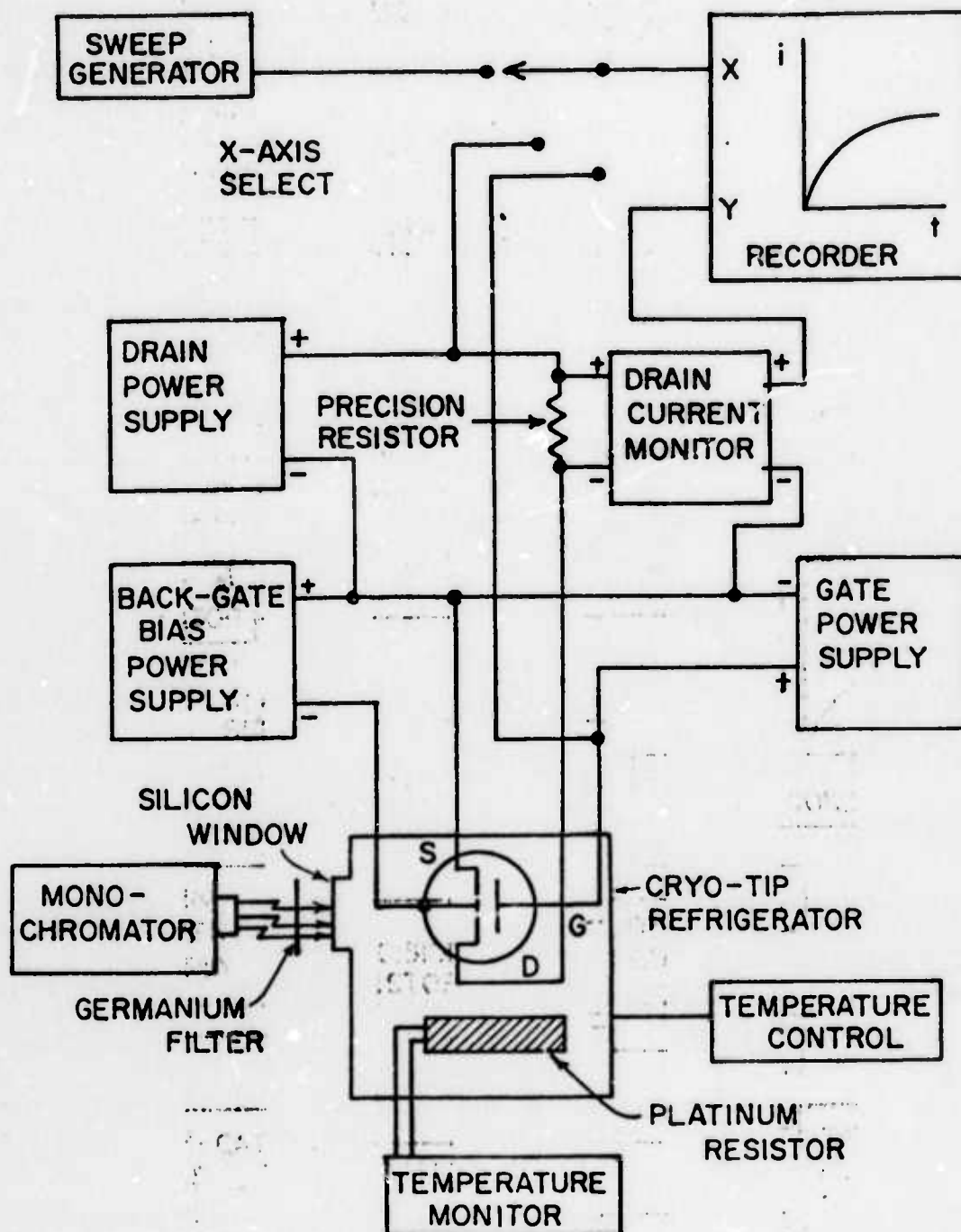72BD, and then employing equation 11 to determine its thickness.

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Figure 4   Flow Chart of the Measurement Technique

OPTICAL RESPONSE

The effect of temperature variation on photocurrent, ΔI_{DS}, has previously been observed [6]. As can be seen from Figure 5, ΔI_{DS} exhibits a similar decay when infrared radiation is incident upon the device. The induim centers were first preset in their neutral charge state by the application of an accumulation voltage. At time $t = 0$, infrared radiation illuminated the device. The resulting decay is due to the photoionization of the indium impurity centers. The time constant of this decay is determined by noting the point where ΔI_{DS} is $\exp(-1)$ times its initial value. As stated previously, $e^o > > e^t$ at the temperature of operation and the resulting time constant is related to e^o through equation 1. The expression for e^o now becomes

$$e^o_p = \sigma^o(\hbar\omega)\phi \; , \tag{16}$$

where $\sigma^o(\hbar\omega)$ is the photoionization cross-section and ϕ is the incident photon flux in number per unit area per second.

The photoionization cross-section, a measure of the probability that a carrier will be emitted due to incident illumination, can be determined by observing the optical decay time as a function of the wavelength of the incident infrared radiation [10]. For a constant photon flux over the wavelength range of interest, equation 16 can be employed to calculate the resulting photoionization cross section. The experimentally determined photoionization cross-section for our experimental device is shown in Figure 6. The units are relative since the measurements were not calibrated in terms of absolute photon flux. This is a very difficult procedure since many reflections exist within the IRFET sample holder. Even leading optical laboratories still have quite a problem in being consistent with their determination of optical flux [11]. However, the measurements were corrected in terms of the spectral characteristics of the monochromator.
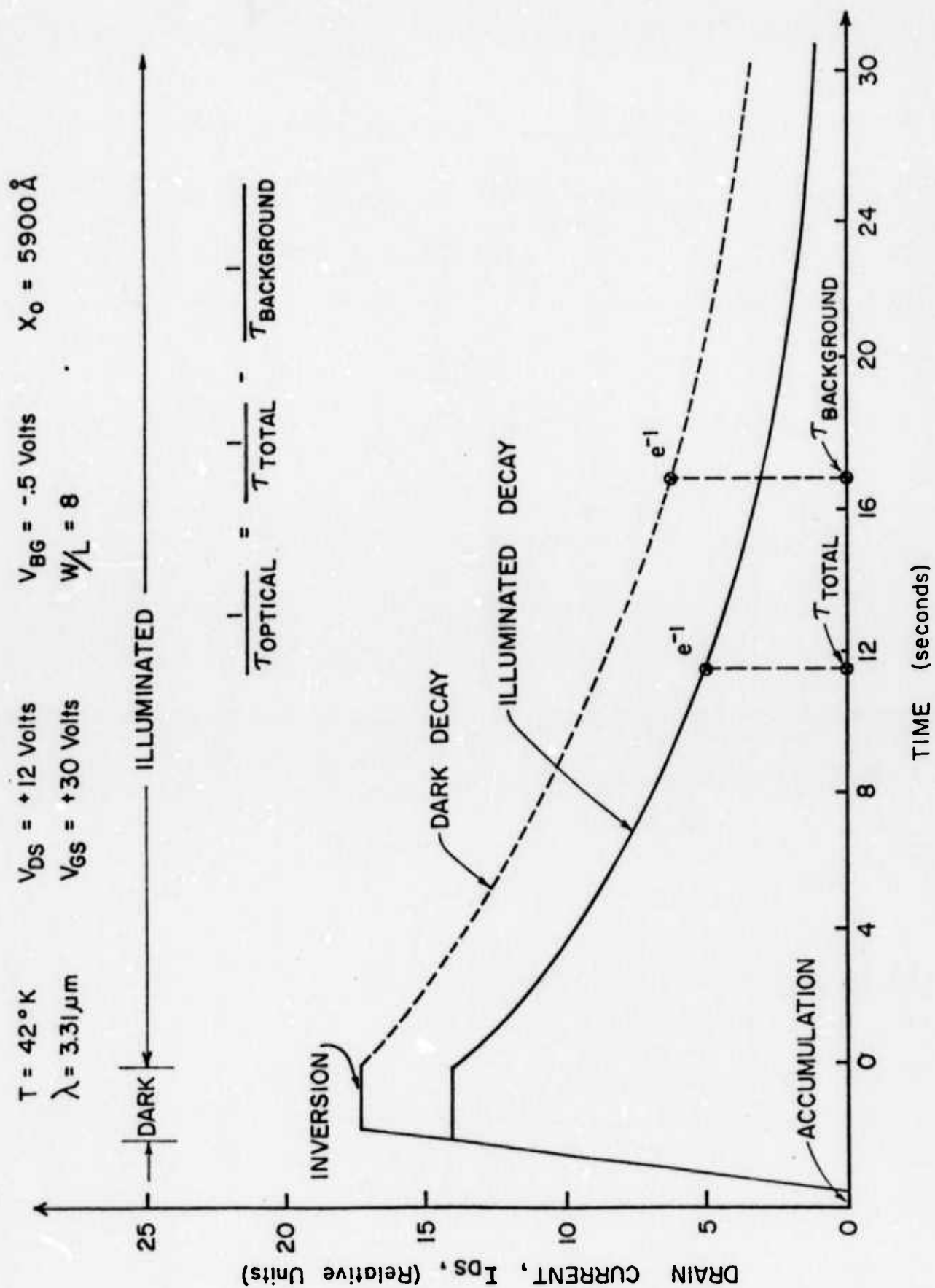
Figure 5 The Transient Decay of Drain Current Due to Incident Infrared Radiation
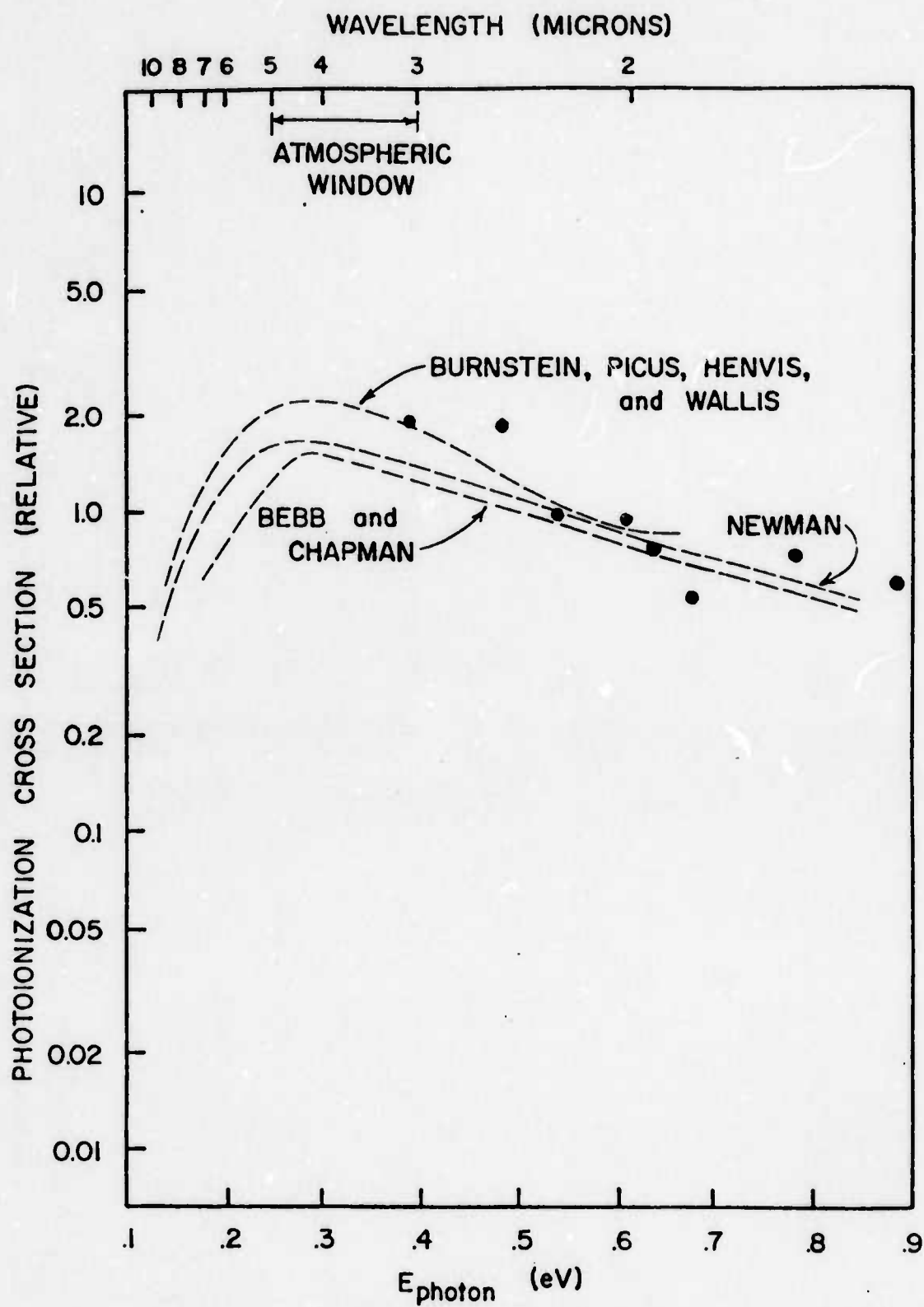
Figure 6   The Photoionization Cross Sections of
Indium in Silicon

Also shown in Figure 6, in comparison to our results for the indium center in the surface depletion region of a MOSFET, are results obtained by other authors for the indium center in bulk silicon [12, 13, 14]. A likely calibration point of .6 eV was used for comparison purposes.

At this time, our determination of photoionization cross-section extends only out to 3.1 microns. This is due to the limit of 3.2 microns on the present monochromator. However, a GCA/McPherson, .3 meter scanning monochromator has been obtained that should extend our graph out to 8 microns. Due to the narrow bandwidth of this monochromator our experimental method will need to be revised so that the output flux of the monochromator will overcome the background radiation that our device is subjected to. The background flux was calculated to be approximately $3x10^{14}/cm^2$-second by observing the "dark" decay time.

OPERATIONAL VERIFICATION

The experimental I-V characteristics of the IRFET are shown in Figure 7. The solid lines correspond to the case where the indium centers are neutral (preset condition) and the dashed lines to the case where the indium centers are negative (after photoionization). As predicted by equations 12 and 13, the current does indeed decrease in the IRFET after illumination with infrared radiation. The ideal MOSFET equations, equations 9 and 10 were evaluated at several points on this graph in order to determine an average surface electron mobility that could be used in the device equations to model the IRFET. A value of 1232 cm^2 per V-sec. was obtained for the mobility. This large value of mobility suggests that the lattice scattering has been greatly reduced at this temperature of operation [15].

The IRFET photocurrent, $-\Delta I_{DS}$, is shown plotted in figure 8 as a function of V_{GS} in the linear region. The theoretical expression for photocurrent, equation 12, suggests no variation in $-\Delta I_{DS}$ as V_{GS} is varied, as is indicated

$X_0 = 5400 \text{ Å}$ $T \approx 42°K$

$W/L = 8$ $V_{BG} = -3V$

$V_{GS} = {}^+16V$

$V_{GS} = {}^+14V$

$V_{GS} = {}^+12V$

$V_{GS} = {}^+10V$

I_{DS}^i (mA)

V_{DS} (Volts)

$X_0 = 5400 \text{ Å}$ $T \approx 42°K$

$W/L = 8$ $V_{BG} = -3V$

$V_{GS} = {}^+16$

$V_{GS} = {}^+14V$

$V_{GS} = {}^+12V$

$V_{GS} = {}^+10V$

I_{DS}^f (μA)

V_{DS} (Volts)

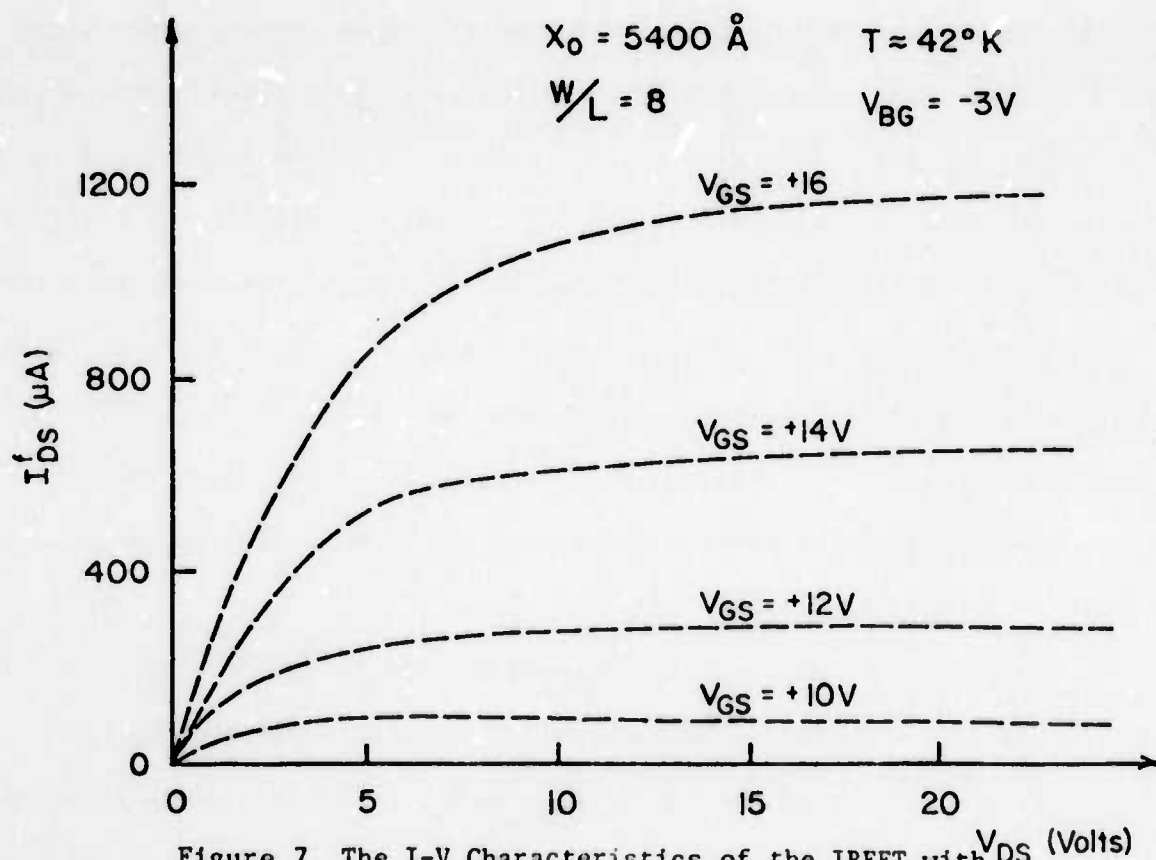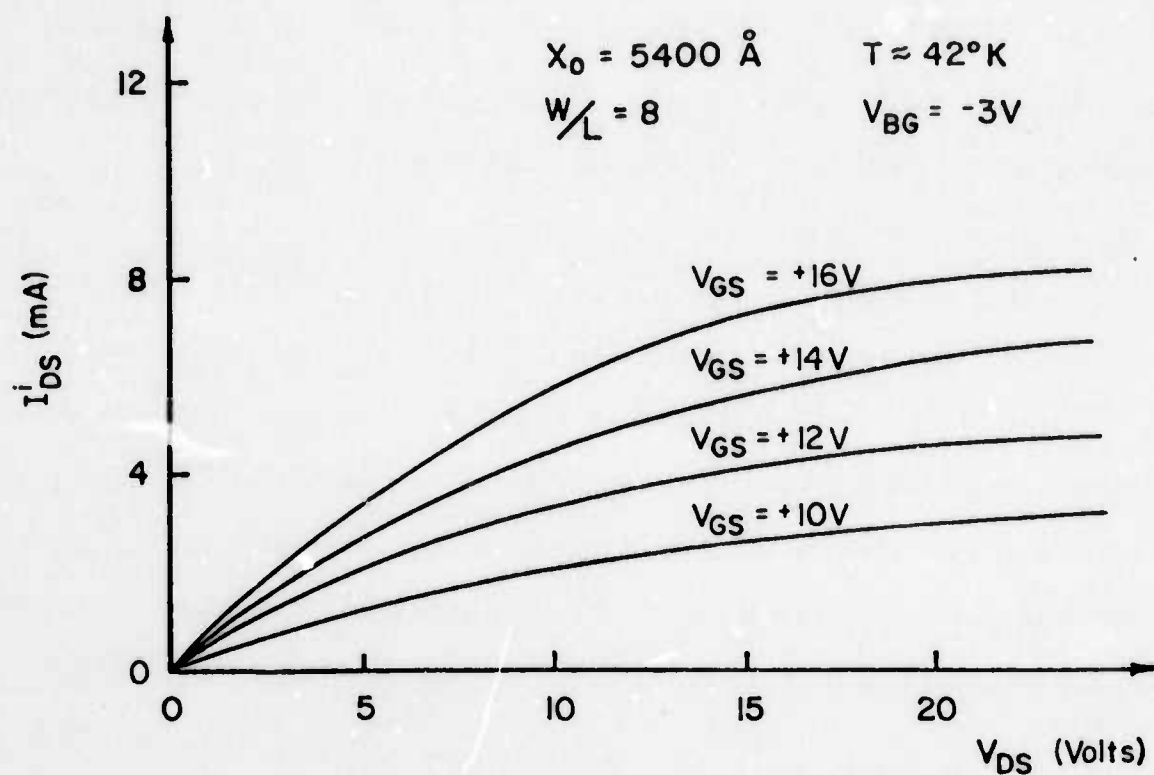Figure 7 The I-V Characteristics of the IRFET with the Indium Center Neutral (solid lines) and Negative (dashed lines)
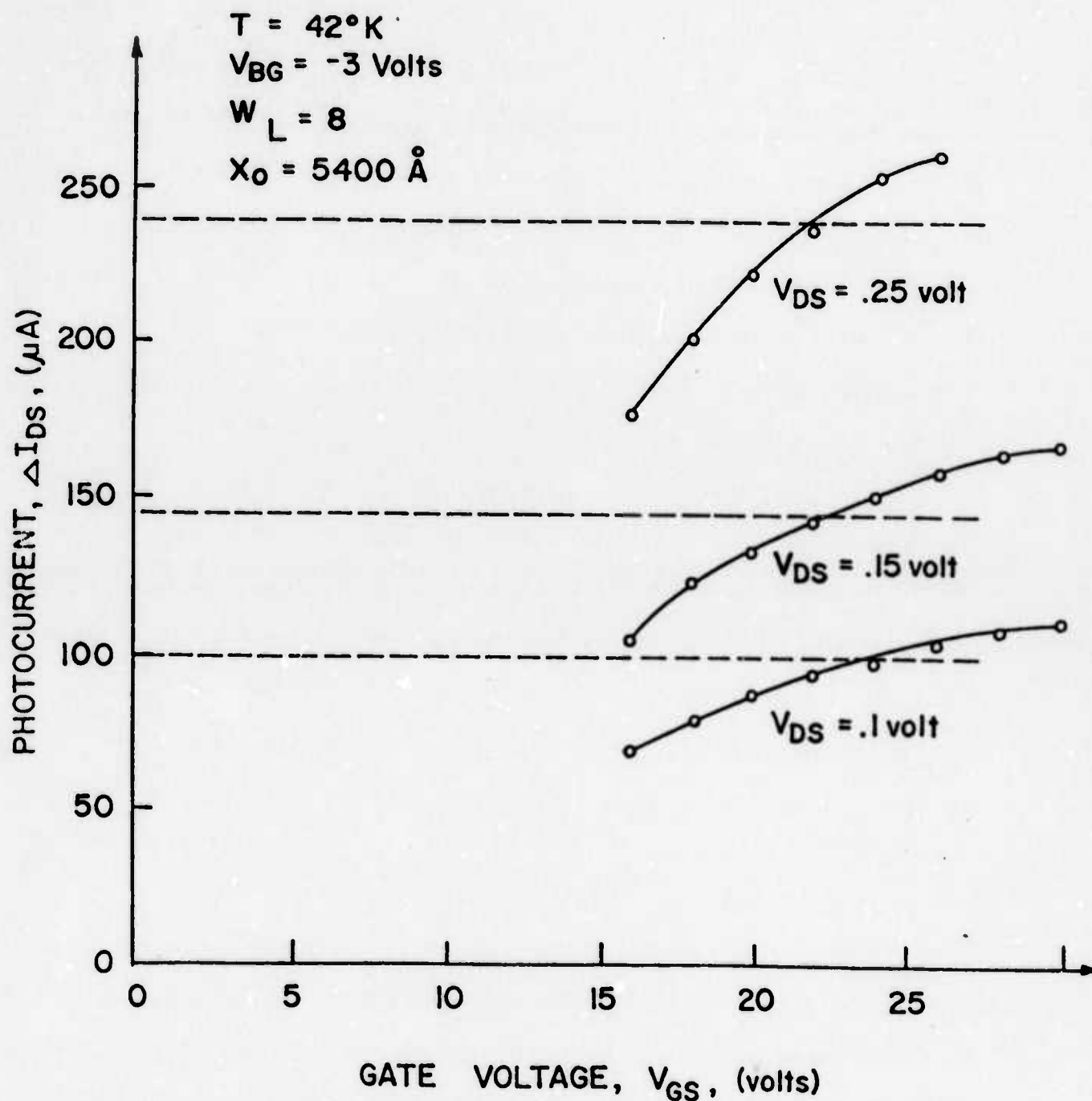
LINEAR REGION

Figure 8   The Photocurrent as a Function of Gate Voltage
in the Linear Region

by the dashed lines of the figure. However, the ideal MOSFET equations, from
which equation 12 was derived, assumes that the drain to source current is zero
when the applied gate voltage is less than or equal to the device threshold
voltage. In order to make the equations correct, the residual drain to source
current present at $V_{GS} = V_T$ would have to be utilized to modify the MOSFET
equations. This can be done by replacing I_{DS} with $I_{DS}^i - I_{DS}^T$, where I_{DS}^i is the drain
to source current observed before illumination and I_{DS}^T is the residual drain to
source current. In figure 9, I_{DS} versus V_{GS} is plotted in the linear region
for both the indium center neutral and negative. By employing the ideal MOSFET
equation in this region, equation 9, we note that $V_{GS} = V_T + V_{DS}/2$ when $I_{DS} = 0$.
The change in threshold voltage, ΔV_T, can then be determined directly from figure
9 by noting that $V_T^i = 5.8 - .075 = 5.73$ volts and $V_T^f = 18.48 - .075 = 18.4$ volts.
ΔV_T is therefore equal to 12.67 volts.

The photocurrent in the saturation region of operation is shown plotted
as a function of gate to source voltage in figure 10. This curve follows closely
the functional form suggested by equation 13. The linear portion of the curve
is shown extrapolated to $V_{GS} = V_T^i + \Delta V_T/2 = 6$ volts when $\Delta I_{DS} = 0$. The initial
threshold voltage was determined from figure 7 by plotting the $\sqrt{I_{DS}^i}$ versus
V_{GS} for a particular V_{DS}. According to equation 10, the intercept on the V_{GS}
axis will directly yield V_T^i as is shown in figure 11. Solving for ΔV_T yields

$$\Delta V_T = 2(V_{GS} - V_T^i) = 2(6 - .15) = 11.7 \text{ volts,} \qquad (17)$$

which is in good agreement with the value of ΔV_T determined from the linear
characteristics of the IRFET. The theoretical value of the change in threshold
voltage between the two charge states may now be determined. With $N_A = 2.6 \times$
$10^{13}/cm^3$ and $N_{In} = 1.6 \times 10^{16}/cm^3$, equation 6 gives us a predicted value of
$\Delta V_T = 18.7$ volts, which is also in good agreement with both of our experimentally

-26-
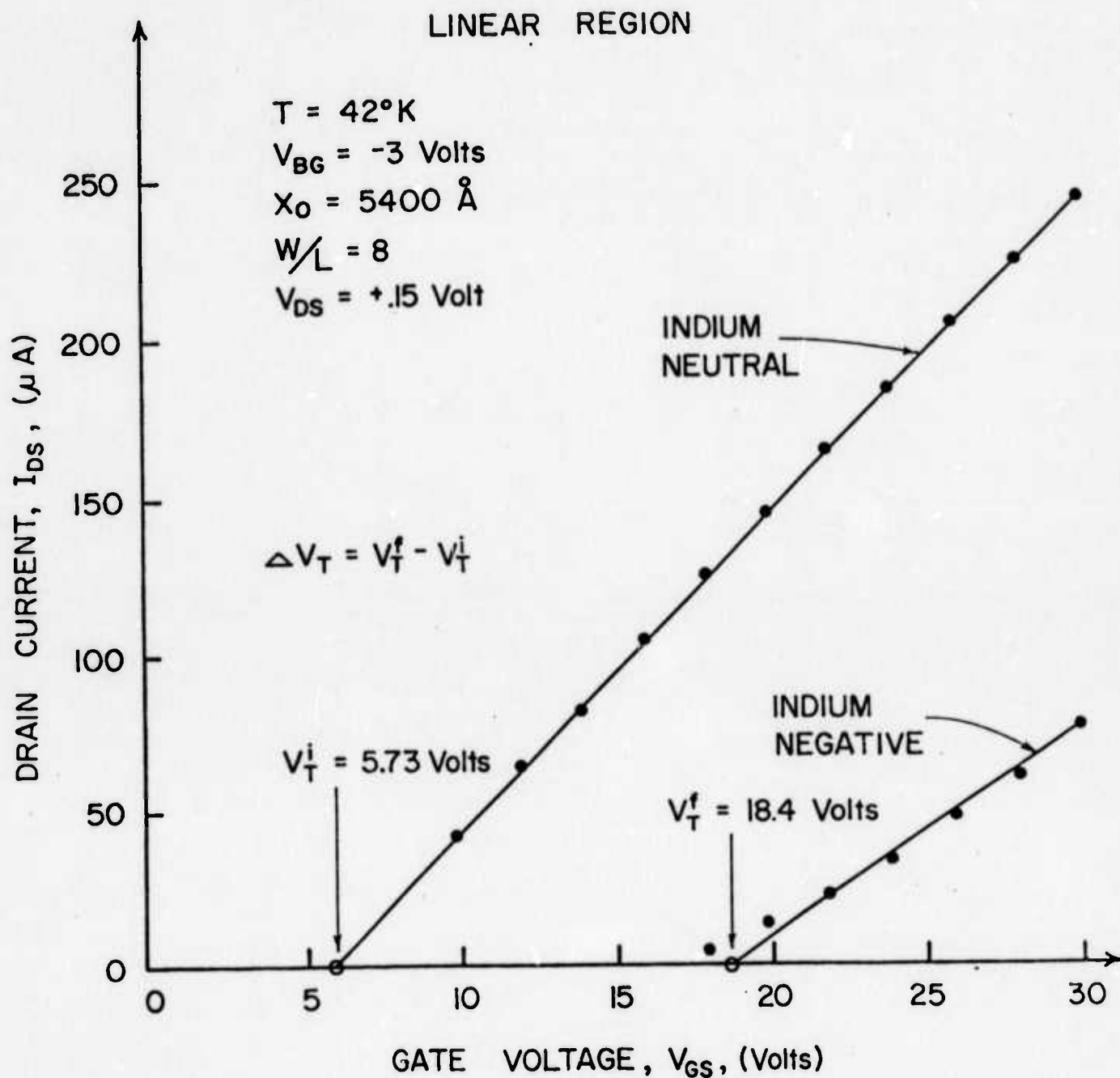
Figure 9 The Determination of the Change in Threshold Voltage,
ΔV_T, From a Plot of Drain Current as a Function of
Gate Voltage in the Linear Region

Figure 10 The Determination of the Change in Threshold Voltage, ΔV_T, From a Plot of Photocurrent, ΔI_{DS}, as a Function of Gate Voltage in the Saturation Region
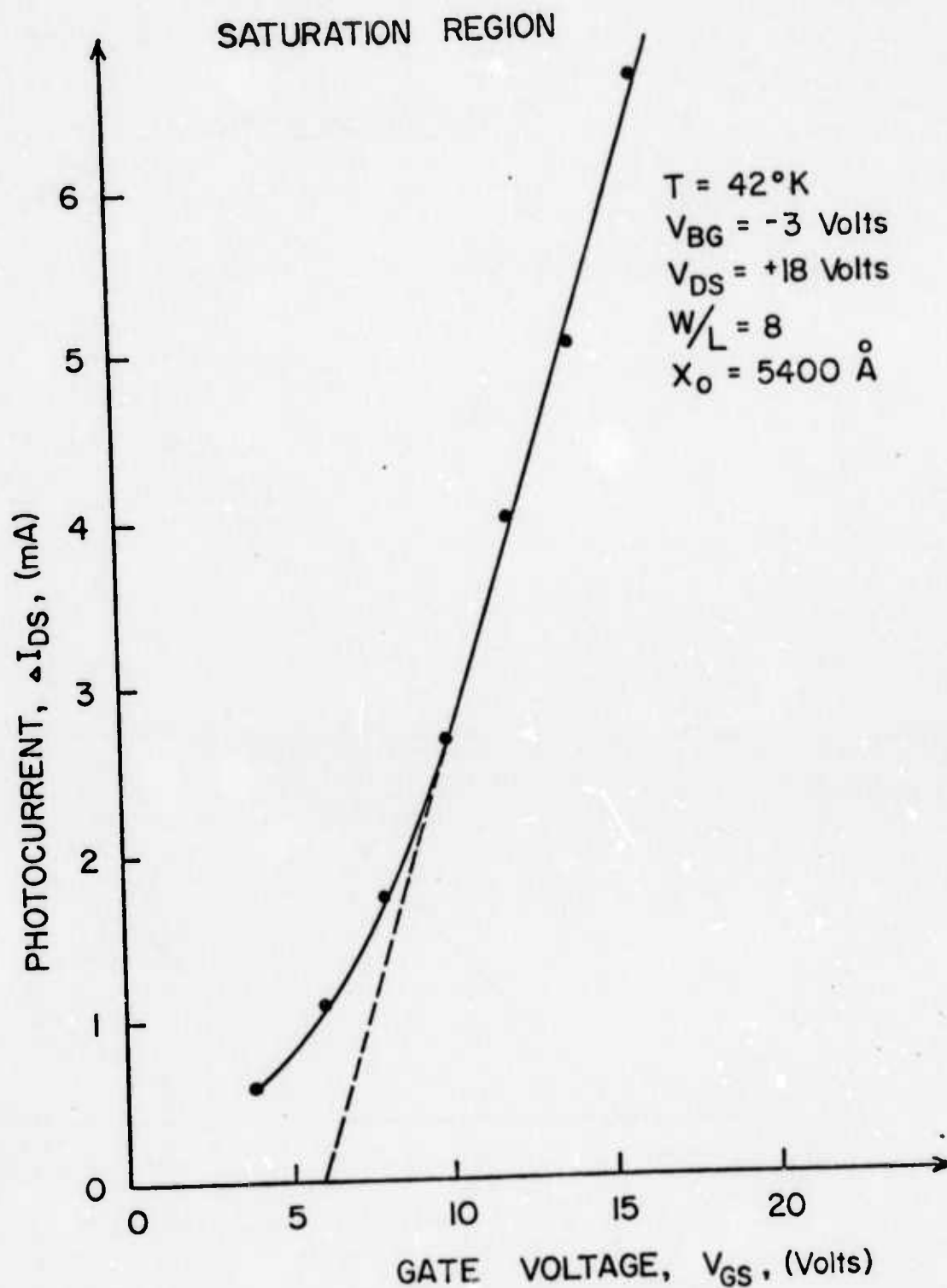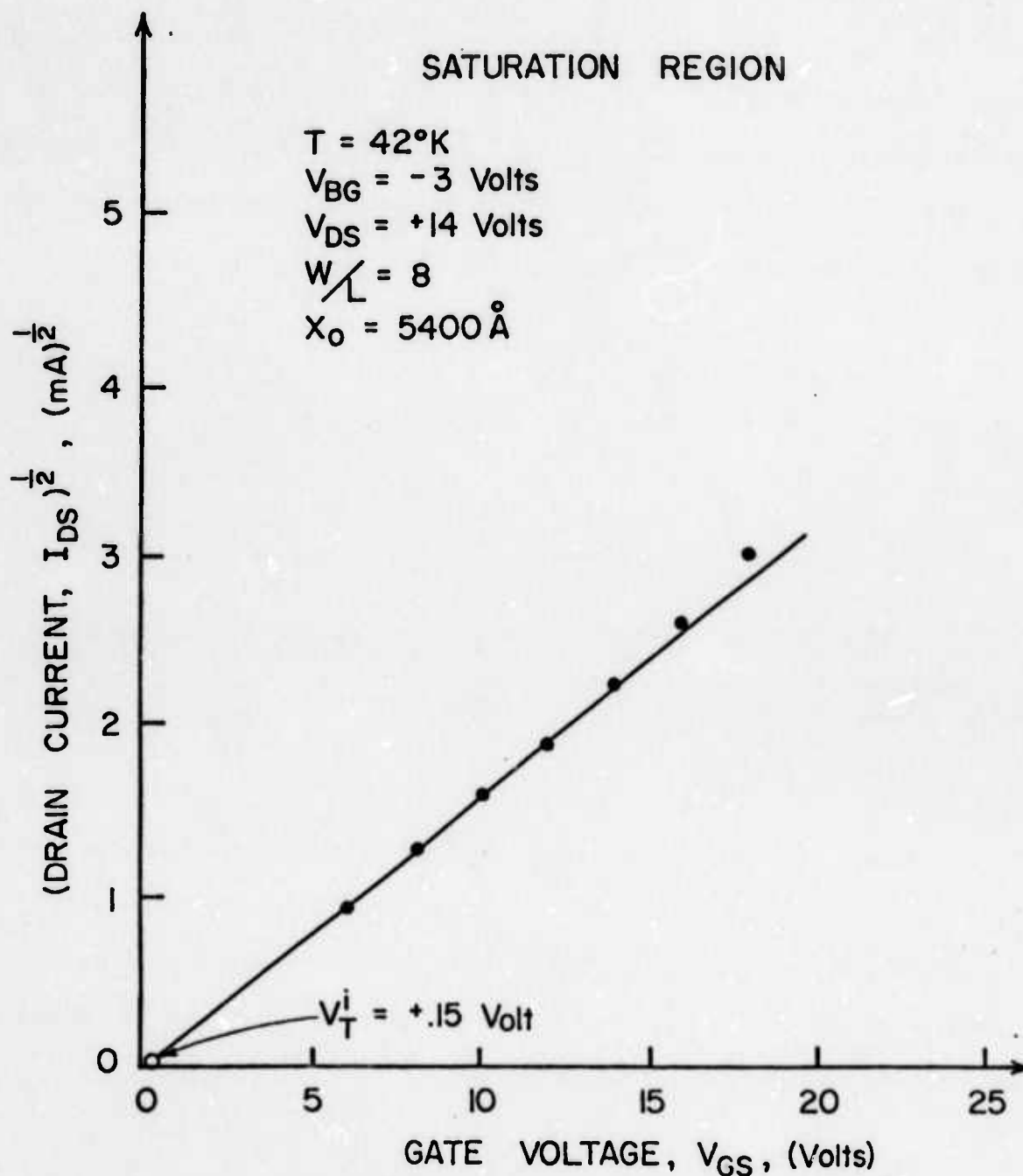
Figure 11   The Determination of the Initial Voltage, V_T^i, from a Plot of the Square-Root of Drain Current as a Function of Gate Voltage in the Saturation Region

-29-

observed values. Since the ideal MOSFET equations exhibit their greatest degree of error in the saturation region, the above results strengthen the credibility of our mathematical model.

The impurity concentrations used above were determined experimentally from a plot of $\sqrt{V_{GB}}$ versus V_T. If we assume that the surface potential, $\phi_s = 2\phi_f$, is approximately equal to 0 at low temperatures, then from equations 2 and 3, we see that the threshold voltage is a function of back gate bias voltage through the term $\sqrt{V_{BG}}$. Differentiating each term in equation 9 separately, the following relations are obtained;

$$\frac{dV_T^i}{d\sqrt{V_{BG}}} = C \sqrt{N_A} \tag{18}$$

and

$$\frac{dV_T^f}{d\sqrt{V_{BG}}} = C \sqrt{N_A + N_{In}} \ , \tag{19}$$

where

$$C = B/\sqrt{V_{BG}} \ .$$

In figure 12 a plot of V_T versus $\sqrt{V_{BG}}$ has been made for the case when the indium centers are neutral ($N_I = N_A$) and for the case when the indium centers are negative ($N_I = N_A + N_{In}$). From an examination of equations 18 and 19, the effective dopings for both charge states can be determined from the slopes of the lines in figure 12.

IRFET RESPONSIVITY

In order to achieve a high responsivity, the IRFET should be operated in the saturation region where the photocurrent, ΔI_{DS}, is independent of the drain
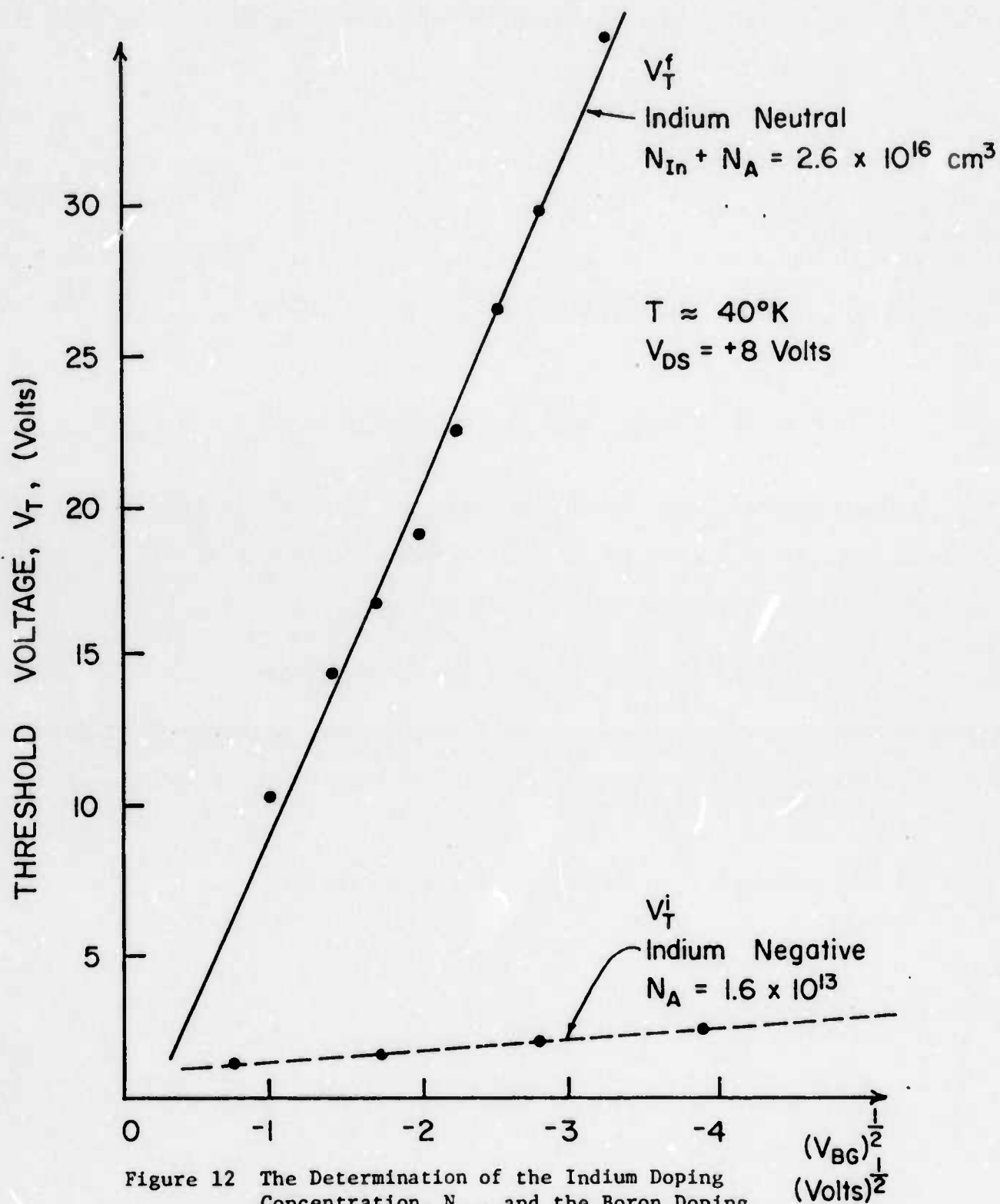
-30-

Figure 12   The Determination of the Indium Doping
Concentration, N_{In}, and the Boron Doping
Concentration, N_A^{In}, for Both the Indium Center
Neutral (solid lines) and Negative (dashed line)
From a Plot of the Threshold Voltage as a Function
of the Square-Root of the Back-Gate Bias Voltage

-31-

to source voltage. Since the IRFET integrates the incident infrared photon flux, an expression for the incident input energy, E_{in}, becomes

$$E_{in} = \phi \cdot t \cdot h\omega \cdot A, \tag{20}$$

where A corresponds to the active area of the device (W·L). At the end of an integration period, t, the drain to source current will have changed by an amount equal to $\Delta I_{DS}(t)$. The expression for the output power, P_{out}, may now be written as:

$$P_{out} = |\Delta I_{DS}(t)| \cdot V_{DS} . \tag{21}$$

The fact that ΔI_{DS} will remain constant until reset and thus can be read for an indefinately long period of time following integration allows us to propose the following definition of IRFET responsivity:

$$\text{RESPONSIVITY} = \text{OUTPUT POWER/INPUT ENERGY.} \tag{22}$$

For illustrative purposes, let us consider the case where the incident infrared radiation is of 2.066 microns. From figure 6, this corresponds to a photoionization cross section of approximately 8.4×10^{-17} cm^2. The device specifications and operating conditions are as follows:

$T = 42^{\circ}K$

$X_o = 5400A^o$

$W/L = 8.17$

$W \cdot L = 2.5 \times 10^{-3}$ cm^2

$V_{DS} = + 18$ volts

$V_{GS} = + 16$ volts

and

$V_{BG} = - 3$ volts.

The decay time constant, τ, was determined experimentally to be 3.35 seconds.

Therefore, by employing equations 1 and 16, a value for the incident photon flux may be determined as follows:

$$\phi = \frac{h\omega}{\tau^o(\sigma^o)} = \frac{h(2\pi)(2.998 \times 10^8/2.066 \times 10^{-6})}{(3.35)(8.4 \times 10^{-17})} = 3.42 \times 10^{-4} \text{ watts/cm}^2 \qquad (23)$$

Employing equation 20 for an integration time much less than τ, such as $\tau/10$, the input energy is found to be 2.86×10^{-7} joules.

For an integration time of $\tau/10$, the photocurrent, ΔI_{DS} was determined to be .86 mA. Therefore, by employing equation 21, the output power becomes,

$$P_{out} = (0.68 \times 10^{-3})(18) = 12.24 \text{ milliwatts.} \qquad (24)$$

The responsivity for this particular case may now be calculated according to equations 22. A responsivity of 42.8 milliwatts per microjoule was obtained.

Much higher responsivities are expected at longer wavelengths since the magnitude of the photoionization cross section peaks between 4 and 5 microns. In addition, since the photocurrent depends only upon the integration time, the effective gate voltage, and the W/L ratio, it will always be the same for the same incident photon flux. However, the output power will increase with increasing V_{DS} and the input energy will decrease as the area (W · L) decreases. Therefore, much higher responsivities can be obtained for smaller devices with a constant W/L ratio.

CONCLUSION

The analytical model of the IRFET, that has been developed, has been shown
to characterize its operation with an appreciable degree of accuracy. The
greatest amount of error is incurred within the ideal MOSFET equations. These
equations were derived by assuming that the surface carrier mobility was in-
dependent of the applied gate voltage and that the net charge in the deple-
tion region, Q_B, was constant along the channel length. Unfortunately, this
is not the case and the equations can be made more representative of the IRFET's
operation if these effects are taken into consideration [8]. However, such
refinements unnecessarily complicate the IRFET model for the degree of accuracy
that is commonly required in most applications.

The basic operating mechanism of the IRFET is impurity photoionization.
If we assume that the charge at the gate electrode and the positive surface-
state charge at the silicon-silicon dioxide interface are fixed, the infrared
detecting capability of the IRFET can be explained simply on the basis of charge
neutrality in the depletion region. Referring once again to Figure 2, the
charge in the surface inversion channel, Q_{CH}, is negative since this is an
n-channel device. Therefore, as Q_B becomes increasingly negative due to the
photoionization of the indium centers, the charge in the channel must become
increasingly less negative. This corresponds to a loss of electrons from the
surface inversion region which results in decreased conductivity between source
and drain and a net decrease in drain to source current.

This new type of infrared detector is an integrating device which exhibits
static read only memory capabilities. Large scale integrated detector arrays
are feasible since the IRFET is based upon existing silicon technology. In
addition, the utility of the IRFET can be extended to the far infrared, the 8
to 14 micron wavelength range, through the use of a gallium dopant as prelimi-

-34-

nary research suggests [1]. It is expected that a simple mathematical model of the gallium-doped MOSFET will be developed which is similar in form to the model presented in this report.

There is considerable scatter in the experimental points in the cross section in Figure 6, as well as extending the measurements to longer wavelengths this work will have to be redone.

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GALLIUM DOPED DEVICES

GALLIUM DOPING BY DIFFUSION FROM DOPED OXIDE SOURCES

INTRODUCTION

The objective of this study was to establish a process for producing double-doped (Gallium and Boron) n-channel MOSFET's. The approach was to begin with p-type boron wafers and diffuse phosphorus for the source and drain regions and Gallium in the channel region under the gate. Gallium diffusion differs from the conventional diffusion process (such as boron and phosphorus) encountered in semiconductor manufacuring in that gallium out diffuses rapidly when silicon is thermally oxidized and silicon dioxide does not mask gallium [1]. The diffusion constant of gallium in SiO_2 is estimated to be a factor of 12 greater than its diffusion constant in silicon [1]. The SiO_2 is therefore transparent to the gallium for practical purposes. The diffusion constant of gallium in silicon is four times that of boron at the same temperature.

Our approach to the problem was to process the boron-doped wafer in the normal manner for producing an n-channel MOSFET until the contact holes are opened. At this point a liquid diffusion source (gallium and silicafilm) is spun over the entire wafer. The wafer is allowed to dry and then subjected to a predeposition drive-in cycle. According to the manufacturer [2], the source produces a co-error function distribution for predeposition time up to one hour [2]. After predeposition, the gallium silicafilm is removed by etching and a drive-in step performed to bring down the surface concentration somewhat and produce a deeper more uniform diffusion profile. It was found that the gallium is violatile at high temperatures and the wafers must be stacked during predeposition to prevent out diffusion. To insure that the gallium does not invert the source and drain regions, a phosphorus source with a surface concentration higher than the solid solubility of gallium is used.

After the drive-in step, the wafer is again etched slightly to remove any oxide formed in the contact holes. The entire wafer is exposed to the final two etchings and gate thickness varies considerably by this process. After etching, aluminum is deposited on the wafer and a masking sequence performed to produce the metal contacts. The devices are now ready for mounting and testing.

The section below describes the experiments performed and the results in establishing the Gallium process.

VERIFICATION OF GALLIUM DOPING

Many MOS capacitors were fabricated on P and on N-type silicon wafers. Gallium was predeposited on the wafer surface for various periods of time. Also the drive in diffusion period was varied. The oxide thickness was varied between $2000A^o$, $3000A^o$ and $4000A^o$. The gallium diffusion in the Si wafer was observed with satisfactory concentrations after the following experiments were performed using N-type Si wafers and then growing $3000A^o$ of SiO_2. Gallium predepositions were carried out at a temperature of 1200^oC. Gallium drive-in diffusions were carried out at a temperature of 1150^oC. Predeposition time periods of 15, 30, and 60 minutes were tried, along with drive in time periods of 30 minutes and 60 minutes.

The object wafer was stacked between two buffer n-type wafers during the predeposition and drive-in periods, to prevent gallium from escaping from the surface during heat treatment.

The result of this experiment was a definite surface inversion; verified by measuring the capacitance characteristics of the capacitor versus voltage. The C-V characteristics corresponded to p-type surface instead of an n-type surface, see Fig. 1.

From the recorded C-V characteristics of the MOS capacitor, Fig. 1, and

from the normalized minimum capacitance versus oxide thickness for ideal MIS diodes under high frequency condition, Fig. 2, determination of the wafer doping after gallium diffusion was possible [1].

$$\frac{C \min}{C_i} = \frac{Cmin}{Cmax} = \frac{118}{125} = 0.944 \tag{1}$$

The oxide thickness can be determined from

$$C_{max} = C_{ox} = \epsilon \epsilon_r \frac{A}{d_{ox}} \tag{2}$$

where, C_{ox} stands for oxide capacitance; A stands for area; d_{ox} stands for oxide thickness; and $\epsilon \epsilon_r$ stands for the premittivity.

The capacitor had a diameter of 40 mils and an area of $(8.107 \times 10^{-3} \text{ cm}^2)$, thus;

$$d_{ox} \simeq \frac{2.83 \times 10^{-15}}{C_{ox}} = 2260 \text{A}^o \tag{3}$$

and from Fig. 2, the doping is

$$N_A \simeq 10^{18} \text{ cm}^{-3} \tag{4}$$

Since the original substrate doping was less than 10^{16} cm^{-3}; then we conclude that the resultant gallium doping is around 10^{18} cm^{-3}.

Al dot 40mil diameter

Al
SiO₂
Gallium diffused
Layer

N-Type

V_G
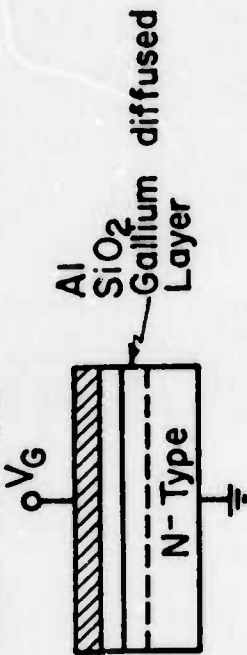
$d_{ox} = 2260\ A°$

$\dfrac{c_{min}}{c_{max}} = 0.94$

$N_{GA} = 10^{18}\ cm^{-3}$

$\dfrac{1}{2}$ hr. Predep at 1200°C

$\dfrac{1}{2}$ hr. drive-in at 1150°C

118 Pf

125 Pf

118 Pf

CAPACITANCE

V_G (Volts)

Fig. 1

-50 -40 -30 -20 -10 0 10 20 30 40 50 60

-47-

Graph axes:
- Y-axis: C'_{MIN}/C_i — values 1.0, 0.1, .01
- X-axis: d(Å) — values 100, 1000, 10,000

Curve labels: $N_A = 1 \times 10^{18}$ cm³, 2×10^{17}, 1×10^{17}, 5×10^{16}, 2×10^{16}, 1×10^{16}, 5×10^{15}, 2×10^{15}, 1×10^{15}, 5×10^{14}, 2×10^{14}, 1×10^{14}
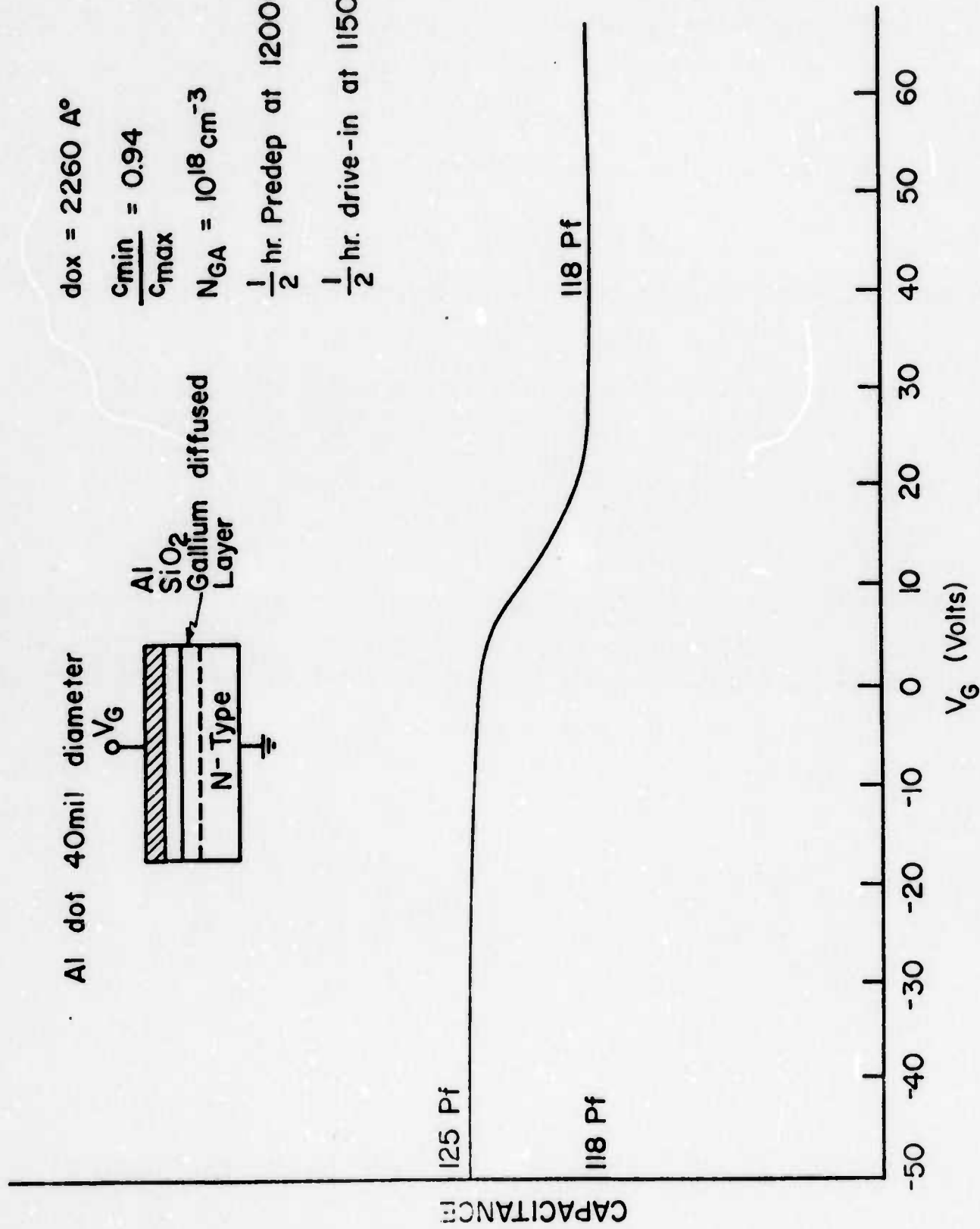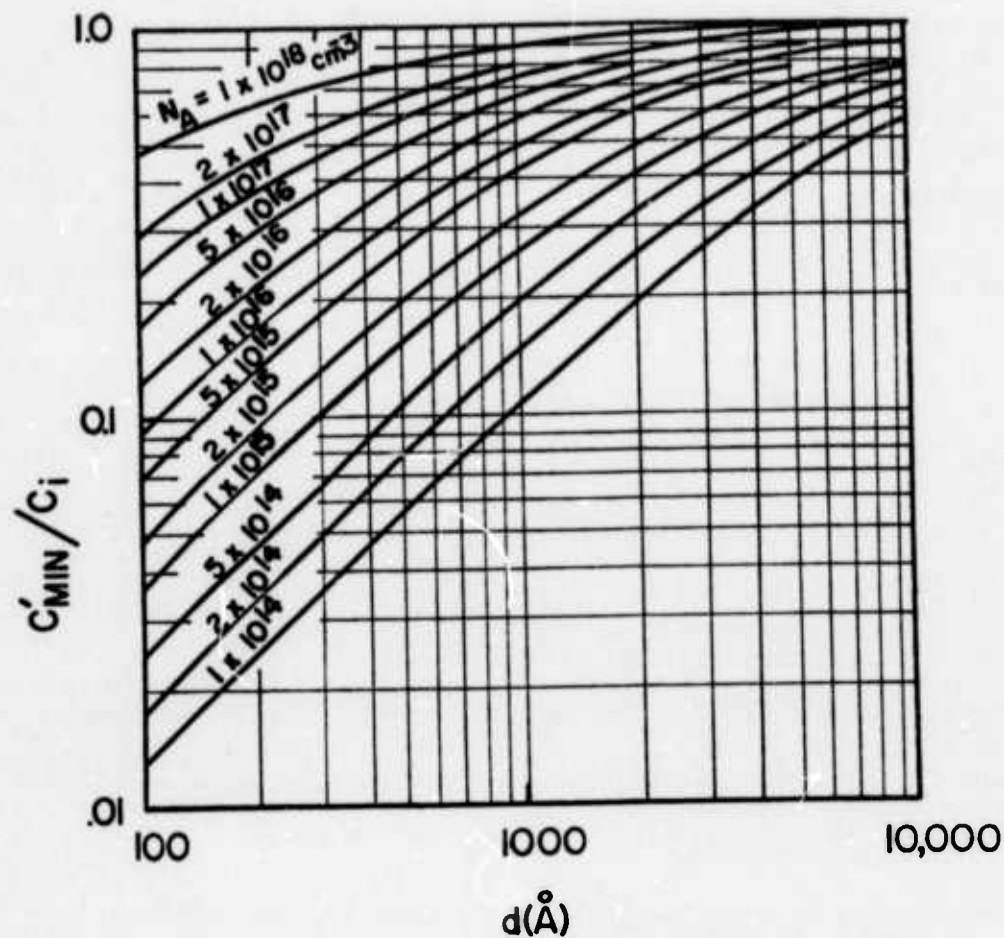
Normalized minimum capacitance versus oxide thickness for ideal MIS diodes under high-frequency condition.

AFTER SZE (4)

FIGURE 2

GALLIUM DIFFUSION PROCESS FOR p-TYPE WAFERS

The following is a description of the fabrication procedure of MOS capacitors and MOSFET's on p-type silicon substrates.

A. Fabrication of MOS Capacitors (Boron, Gallium)

The following is a description of the fabrication procedure for MOS capacitors.

1. Oxide growth (4000A^o SiO$_2$) - See Fig. (3).

   The p-type Silicon Wafer is processed as follows in the oxidation furnace.

   a) 20 Minutes dry oxidation at 1100°c

   b) 60 Minutes wet oxidation at 1100°c

   c) 20 Minutes dry oxidation at 1100°c

   d) 30 Minutes aneal in N$_2$ at 1100°c

2. Coat with Gallium Silicafilm - See Fig. (4).

   The wafer is placed on the spinner. Eight drops of Gallium Silicafilm are deposited on the wafer while spinning at 3000 rpm for ten seconds.

   The film is left to dry at room temperature for one hour.

3. Gallium Diffusion - See Fig. (5) and (6).

   The wafers are stacked and placed in the diffusion furnace.

   a) Predeposition--30 minutes at 1200°c

   b) Remove the Gallium Silicafilm by etching in a buffer solution (1:4 HF:NH4F) for one to one and half minutes

   c) Drive in diffusion--60 minutes at 1150°c

4. Metalization and photolithography to obtain a capacitor with a guard ring for surface accumulation - See Fig. (7).

First Step

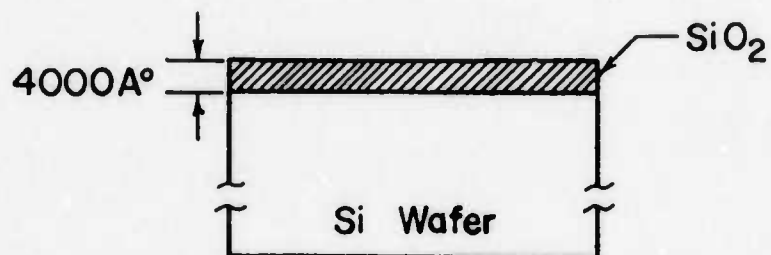FIGURE 3

Second Step

FIGURE 4

Third Step

1200°C

Gal. film →
SiO$_2$ →

Si Wafer
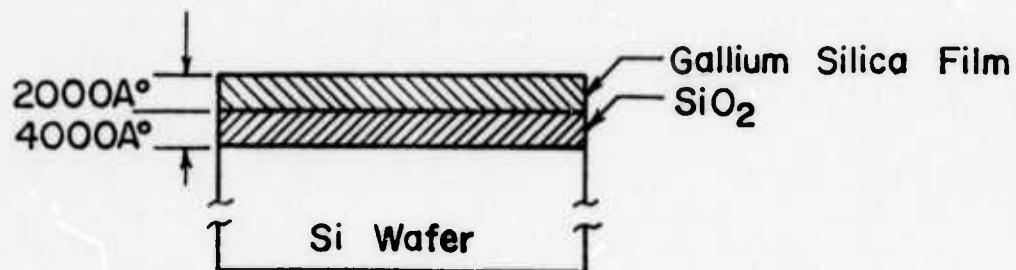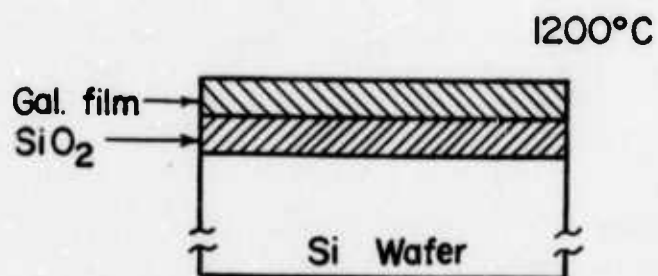
Predeposition at 1200°C for
30 minutes

buffer wafer
of the same type
as the coated waffers
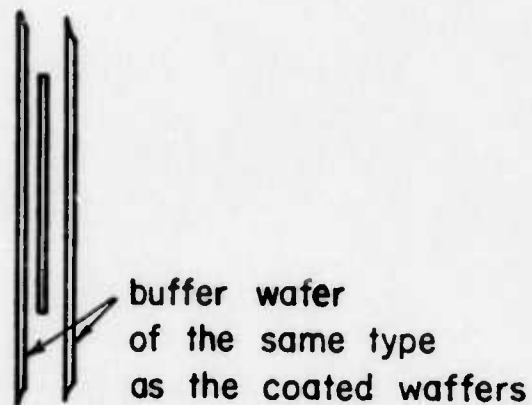
Stacked wafer arrangement
in the diffusion furnace

FIGURE 5

Fourth Step

1150°C

SiO$_2$ →

Si Wafer
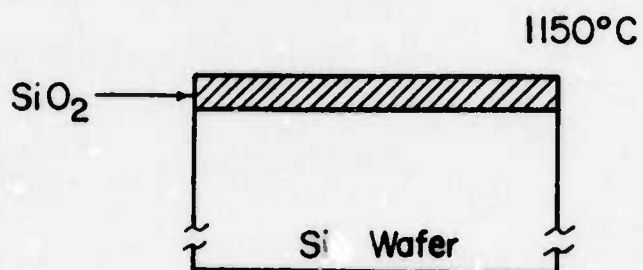
Drive in diffusion for 60 min.

FIGURE 6

Capacitor
ⵁ 40ml

Guard ring for surface
accumulation

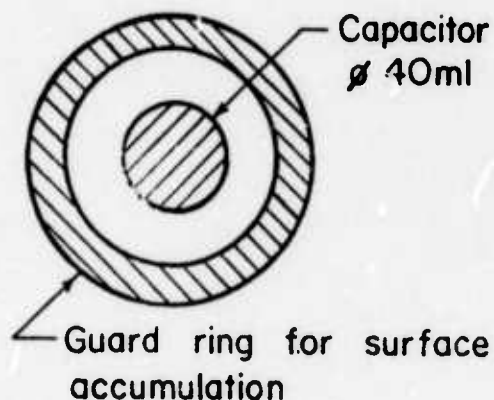FIGURE 7

B. **Fabrication of Double Doped, MOS-FET (Boron, Gallium):**

The following is a description of the manufacturing procedure for MOSFET's.

1. Clean surface of Si-p-type wafer, Boron doped - See Fig. (8).

2. Oxide growth 7000A^o SiO$_2$ - See Fig. (9).

   a. 20 minutes dry oxidation 1100°c

   b. 180 minutes wet oxidation 1100°c

   c. 20 minutes dry oxidation 1100°c

   d. 30 minutes aneal in dry N$_2$

3. Photolithography

   Photoresist masking step to open the source and drain diffusion

   areas in the oxide - See Fig (10).

4. Phosphorus diffusion - See Fig. (11).

   a. Coat the surface of the wafer with phosphorus silicafilm. 4
   to 5 drops of the phosphorus silicafilm on the surface of the
   wafer while spinning at 3000 rpm for ten seconds. (This process
   is repeated two times and the wafer then baked at 200°C for 15
   minutes to dry the phosphorus film.)

   b. Predeposition--one hour at 1100°c

   c. Remove the phosphorus silica film by HF etch

   d. Drive in diffusion--one hour at 1100°c - See Fig. (12).

   e. Etch 4000°A of the oxide without exposing the gate area. (This
   protects the surface and avoids surface inversion during the
   gate oxidation process due to phosphorus evaporation.)

5. Grow 3000°A gate oxide (See step 2) - See Fig. (13).

6. Photolithography

   Photoresist masking step to open the contact holes in the oxide of
   the source and drain regions - See Fig. (14).

7. Gallium Diffusion - See Fig. (15).

   a. Deposit 8 drops of the Gallium silicafilm on the surface of the
      wafer while spinning at 3000 rpm for ten seconds.

   b. Dry the gallium film at room temperature for one hour.

   c. Predeposition - 30 minutes at 1200°c.

   d. Etch the silicafilm.

   e. Drive in diffusion - 60 minutes at 1150°C in dry N_2 with 10% oxygen
      flow.

8. Etch 700A° of SiO_2 from the surface.

9. Metalization and photolithography to establish separate contacts with
   source, drain regions and gate oxide.

The following modifications were also carried out to reduce the number of
gate shorts and to increase the yield of the double doped MOSFET fabrication
process.

1. Sulfuric acid was used to remove any remaining gallium at the surface
   of wafer after the etching step.

2. Growing the gate oxide while driving in the gallium, thus eliminating
   the separate Ga drive in step in the above process. The gate oxide growth
   was carried out as follows:

   15 min. dry oxidation

   60 min. wet oxidation

   20 min. N_2 aneal
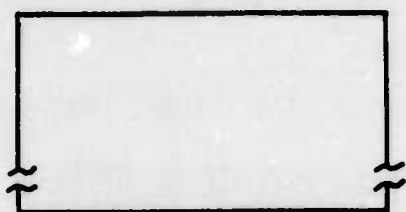
P-type Si Wafer
(Boron doped)

FIGURE 8

7000 A°
oxide
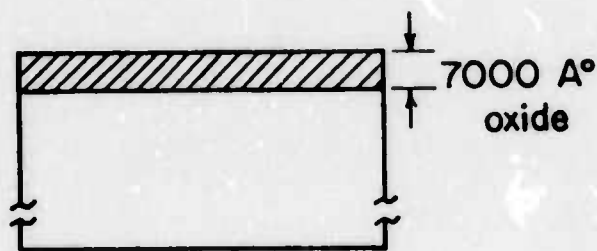
oxide growth

FIGURE 9
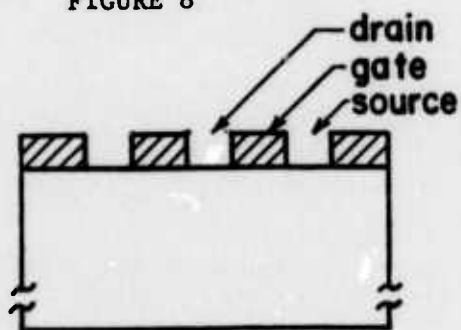
drain
gate
source

Opening the source
and drain regions
in the oxide.

FIGURE 10

SiO$_2$

Phosphorous silica film

FIGURE 11

3000 A°
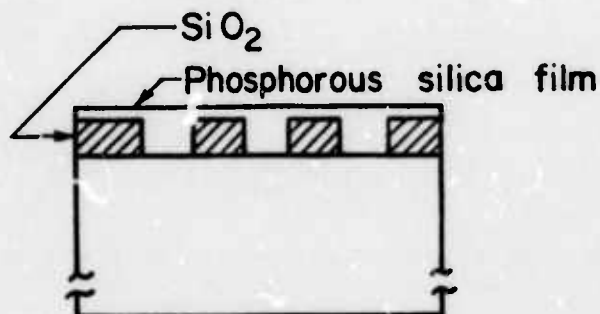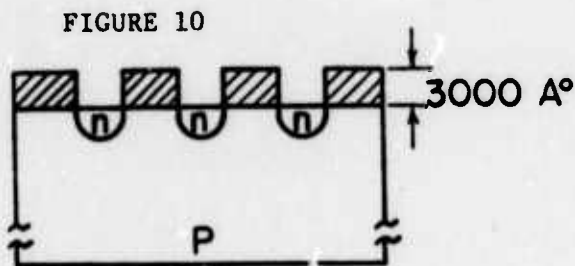
source & drain
regions

FIGURE 12

5000 –
3000 A°
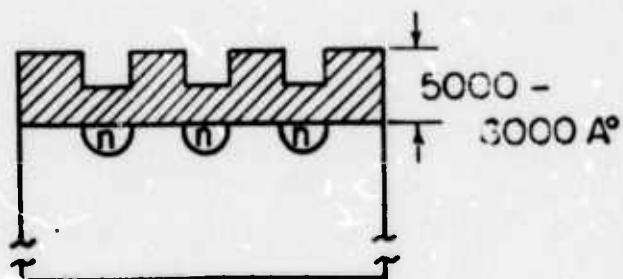
gate oxide

FIGURE 13

-47-
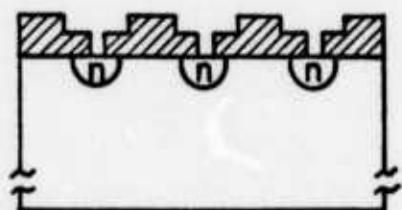
opening contact holes

FIGURE 14

Gallium silica film
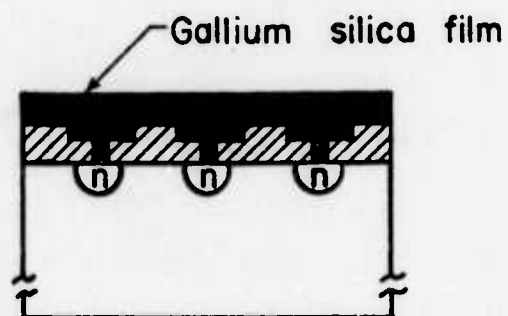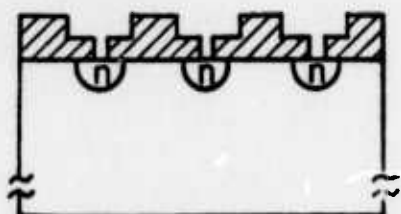
FIGURE 15

the device after
Gallium film predeposition,
etching and drive in

FIGURE 16
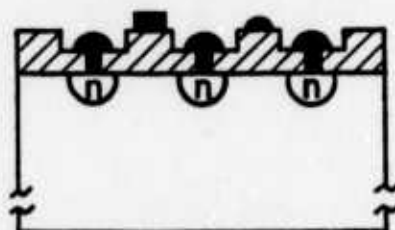
metalization

FIGURE 17

GALLIUM DOPED MOSFET AT ROOM TEMPERATURE

The MOSFET's that were fabricated according to the process described above, were mounted and measured at room temperature. The I-V characteristics of one of them is shown in Fig. 18. By measuring the threshold voltage at various back gate voltages, the Ga concentration was estimated to be $\simeq 10^{17} cm^{-3}$.

CONCLUSIONS

Based on these experiments we conclude that gallium doping of p-type silicon wafers can be achieved by gallium diffusion through an oxide from a doped oxide source.
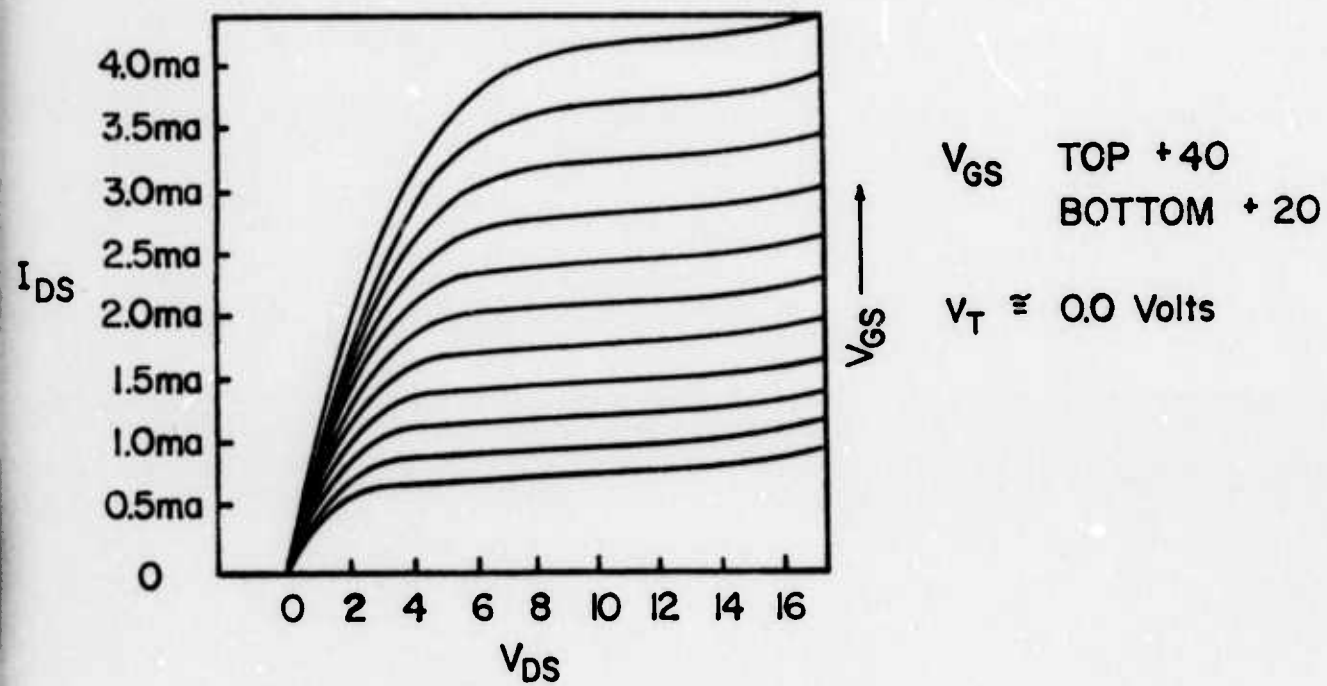
Double doped MOSFET
(Gallium - Boron)

Fig. 18

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PRELIMINARY RESULTS ON OPERATION OF THE GALLIUM DOPED INFRARED SENSING MOSFET

Some preliminary low temperature measurements have been made on the characteristics of the gallium doped MOSFET's described in the previous section. These measurements are similar to those described previously in the section on the experimental verification of the operation of the indium doped infrared sensing MOSFET. Here, however, the ionization energy is smaller and lower temperatures of operation are required.

Fig. 1 shows the curve tracer characteristics corresponding to the two distinctly different charge states of the gallium center. The dashed lines in Fig. 1 correspond to the case where the gallium centers are in the neutral charge state following accumulation of the surface by applying a negative gate voltage. The dark line in Fig. 1 corresponds to the case where the gallium centers have been allowed to emit holes to the valence band and the gallium centers are ionized or in the negative charge state. The increase in the space charge in the surface depletion regions results in an increase in threshold voltage of the MOSFET and consequently a decrease in the conductivity. The observation of two distinctly different conductivity states associated with different gallium charge states essentially amounts to an experimental verification of operation of the gallium doped infrared sensing MOSFET (IRFET).

Fig. 2 shows preliminary results on the measurement of the time constant associated with the thermal emission of holes from the gallium centers. In making these measurements, relatively fast time constants, in the millisecond range, have been employed. Not only are these easier, since they correspond to higher temperatures but it is believed they are more representative of the actual operating conditions under which the IRFET might be employed. The gallium doped devices are anticipated to have a peak optical response in the 8 to 14 micrometer wavelength range. At these wavelengths the signal or photon

GALLIUM-BORON DOPED MOSFET

$V_{BG} = 0.0$ VOLTS

$T \cong 24.5\,°K$
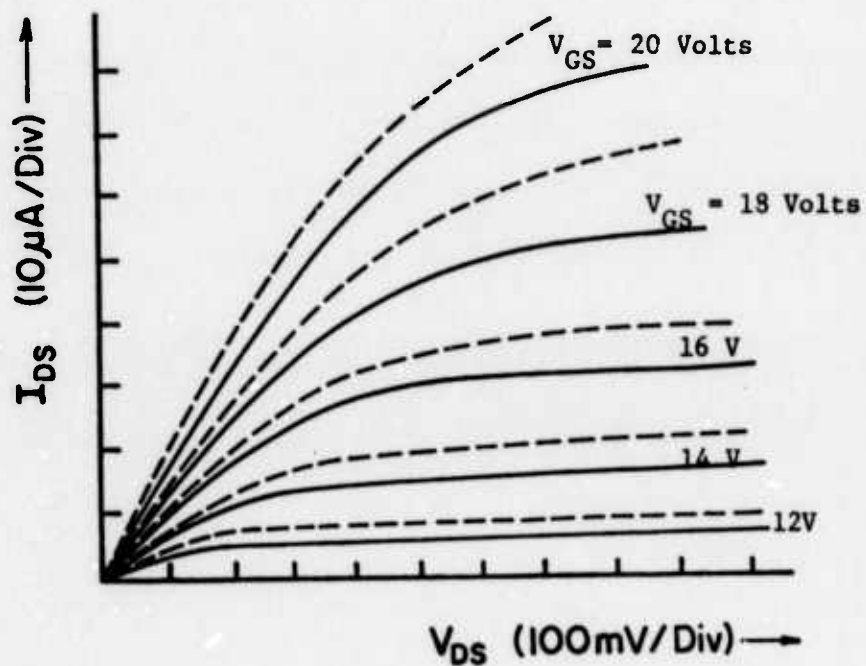
Fig. 1 I-V Characteristics of a double doped, gallium and boron doped,
infrared sensing MOSFET (IRFET). Dashed lines, gallium neutral;
solid lines, gallium negative charge state.

flux from a 300°K blackbody source is very large and consequently under normal operating conditions the signal photon flux incident on the detector is very large. This would result in relatively speaking fast discharge times for the gallium centers.

Also shown in Fig. 2 are our previous results for the gold donor and indium levels in silicon. The time constant associated with the decay is the reciprocal of the thermal emission rate, and the slope of the lines are proportional to the ionization energy of the impurity center. A relatively strong field dependence has been observed in the thermal emission rate for holes from the gallium center.

All aspects discussed and presented in this preliminary report on the gallium center are currently under further investigation.

Fig. 2 Time constants associated with thermal emission of holes from the gallium, indium and gold donor levels.
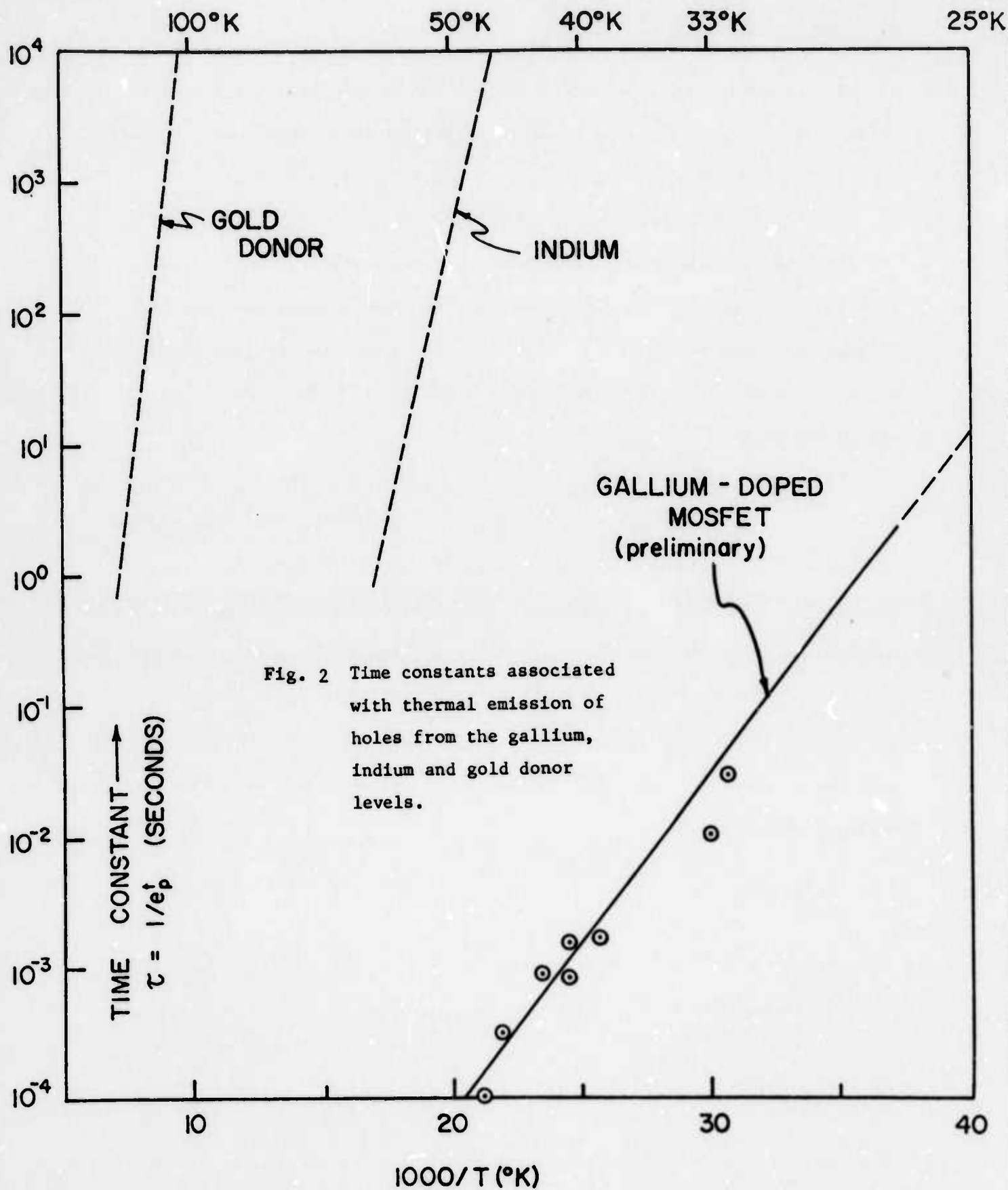
APPLICATION CONSIDERATIONS & NOISE

The report on the considerations involved in the application of the IRFET as an infrared detector is divided into two parts, these are

(i) Theoretical Background Limited Operation of Solid-State Infrared Detectors and Imaging Arrays.

(ii) Noise Measurements on Infrared Sensing MOSFET's.

In the first, it is shown that ALL surface type solid-state infrared imaging detectors theoretically have essentially the same maximum obtainable signal to noise ratio. This limit is imposed by shot noise due to the background flux.

In the second, measurements have been made to identify the dominant noise mechanisms in the IRFET. It has been observed that two noise sources are important, shot noise, and 1/f noise. It has been shown that shot noise exceeds 1/f noise for a wide range of operating conditions, namely for the shorter integration periods and higher photon fluxes, indicating that the IRFET could indeed be operated under background limited conditions.

To facilitate discussion of the theory and experiments on noise, a list of symbols follows defining the variables employed, along with their corresponding units.

LIST OF SYMBOLS

A	Area of individual detector, $cm.^2$
A_{IP}	Area of image plane, $cm.^2$
BW, ν	Bandwidth, $sec.^{-1}$
C_o	Oxide or insulator capacitance, farads $cm.^{-2}$
$D*$	Detectivity, $cm. \ sec^{-\frac{1}{2}} \ watt^{-1}$
e_o	Electric permittivity of free space, farad $cm.^{-1}$
e_p^o	Optical emission rate, $sec.^{-1}$
$\hbar w_s$	Signal photon energy, joules
$(\overline{i_N^2})^{\frac{1}{2}}$	Root mean square (rms) noise current, amps.
$(\overline{i_{DSN}^2})^{\frac{1}{2}}$	rms drain to source noise current, amps.
$\overline{I}$	Mean or average current, amps.
I_{DS}	Drain to source current, amps.
K_s	Relative dielectric constant of silicon
K_o	Relative dielectric constant of oxide
L	Channel length, cm.
n	Number of points in image
N	Background photon flux, $sec.^{-1} \ cm.^{-2}$
N_A	Acceptor impurity concentration, $cm.^{-3}$
NEP	Noise equivalent power, watts
N_S	Surface charge density, $cm.^{-2}$
N_{TT}	Impurity concentration, $cm.^{-3}$
q	Electronic charge, coulombs
Q_{CH}	Charge in channel, coulombs
$(\overline{Q_N^2})^{\frac{1}{2}}$	rms variation in charge , coulombs

T_I	Integration Time, sec.
T_F	Frame time, sec.
T_S	Sample time, sec.
S/N	Signal to noise ratio
V_{BG}	Back gate or substrate bias, volts
V_{DS}	Drain to source voltage, volts
V_{GS}	Gate to source voltage, volts
V_T	Threshold voltage, volts
W	Gate or channel width, cm.
W_d	Depletion region width, cm.
x_o	Oxide thickness, cm.
Δ	Indicates change in quantity following symbol
η	Quantum efficiency
μ	Mobility, $cm.^2$ $volt^{-1}$ $sec.^{-1}$
σ	Photoionization cross section, $cm.^2$
τ	Time constant, sec.
ϕ_f	Fermi potential, volts.
ϕ	Signal photon flux, $sec.^{-1}$ cm^{-2}
ψ_s	Surface potential, volts

THEORETICAL BACKGROUND LIMITED OPERATION OF SOLID-STATE INFRARED DETECTORS AND IMAGING ARRAYS

INTRODUCTION

The ability of infrared imaging arrays to detect signals from the desired scene is limited in terrestial applications by the noise resulting from the background illumination assuming that this background radiation is uniform. Historically, of course, the simplest technique for infrared imaging has been to mechanically scan the scene across a single detector of area, A, where the bandwidth, BW, of the signal amplification system is determined by the number of points in the scene and scan rate. This leads to the definition of a relative figure of merit for comparing detectors as the detectivity or $D* = (A)^{\frac{1}{2}} (BW)^{\frac{1}{2}}/NEP$, where NEP is the noise equivalent power. [1]. This concept is in reality, however, only useful for the classical system where the scene is scanned across a single detector or line array of detectors. In the case of the newer types of devices as for instance, charge-injection diodes, CID's, [2,3], charge-coupled devices, CCD's, [3,4,5] or infrared sensing field effect transistor's, IRFET's [6,7,8] there is no well defined single bandwidth but on the other hand two bandwidths, one associate with the integration period, T_I, and one associated with the sample period, T_S.

The objective of this report is to consider the more general case and specifically derive the noise equivalent signal power, NEP, for arrays of CID's or CCD's, and IRFET's employed in infrared imaging arrays. This is particularly relevant since concern has been expressed over saturation effects in these devices due to background radiation, [3,4], it will be shown however, that the NEP for these types of imaging arrays can be orders of magnitude smaller than for a single photodiode or photoconductor system. This would thus allow the use of large F/number or narrow bandwidth optical systems and consequently orders of magnitude less background radiation incident on the array. This low NEP results from

the much smaller effective bandwidth if large number of integrating detectors are employed rather than a single detector.

Since we are dealing with the theoretical limit on the operation of infrared imaging detectors due to background radiation it will be assumed that the dominant noise mechanism is shot noise due to this background. Photon noise will not be considered since it only introduces a small additional factor similar to the shot noise, [1] and other types of noise as 1/f, Johnson, and generation-recombination will also not be considered. Each of the three different types of imaging techniques will be treated separately where the area of the scene in the image plane, A_{IP}, and frame time, T_F, background photon flux, N, number of points or elements in the scene, n, quantum efficient, η, and signal photon energy $\hbar w_s$ are the parameters for the imaging application.

MECHANICALLY SCANNED SINGLE PHOTODIODE OR PHOTOCONDUCTOR

This is the classical case and the NEP for a single detector [1] is

$$NEP = \hbar w_s (2N \ A \ BW/\eta)^{\frac{1}{2}} \tag{1}$$

however, the area of the detector in an imaging application must be $A = A_{IP}/n$ where n is the number of elements in the scene and the bandwidth of the system must be large enough to accomodate these n data points in the frame time. Therefore, $BW = n/T_F$ and then:

$$NEP = \hbar w_s (2N \ A_{IP}/\eta \ T_F)^{\frac{1}{2}} \tag{2}$$

watts for each point in the scene. This is the total amount of power which must be received from the scene over an area A, of the detector, for the signal to be comparable to the shot noise.

INTEGRATING DYNAMIC CHARGE STORAGE DEVICES, CID's, or CCD's

Suppose an array of CID's [2, 3] or CCD's [4, 5] is fabricated on an extrinsic semiconductor and employed in an imaging application. Each of these

n elements will integrate the photocurrent over the frame time and then be read out during some sample period, $T_S = T_F/n$, so that all can be read for each frame. If the quantum efficiency is η, then the average photocurrent in each detector of area A is, $\overline{I} = q\eta AN$, this will result in a mean square noise current given by Carson's Theorem as

$$\overline{i}_N^2 = 2q\,\overline{I}/T_I = 2q^2\eta A\,N/T_I \tag{3}$$

This will further result in an uncertainty in the charge stored by each detector at the end of the integration period of

$$(\overline{Q}_N^2)^{\frac{1}{2}} = (\overline{i}_N^2)^{\frac{1}{2}}\,T_I = (2q^2\eta A\,NT_I)^{\frac{1}{2}} \tag{4}$$

when this charge is read out the root mean square noise current in the sample period, T_S, will be

$$(\overline{i}_N^2)^{\frac{1}{2}}{}_{sample} = (\overline{Q}_N^2)^{\frac{1}{2}} / T_S \tag{5}$$

$$(\overline{I}_N^2)^{\frac{1}{2}}{}_{sample} = (2q\,\overline{I}T_I/T_S^2)^{\frac{1}{2}} \tag{6}$$

On the other hand the signal will result in a photocurrent in the sample period of

$$i_{signal} = q\eta A\,\Phi\,T_I/T_S. \tag{7}$$

Equating these two yields the signal flux, Φ/cm^2 sec., corresponding to the NEP and then,

$$NEP = \hbar w_s\,(2N\,A/(\eta T_I))^{\frac{1}{2}}\,watts \tag{8}$$

In the imaging application, $A = A_{IP}/n$, $T_I = T_F$, and

$$NEP = \hbar w_s\,(2N\,A_{IP}/(\eta\,T_F\,n))^{\frac{1}{2}}\,watts \tag{9}$$

for each point in the scene. Obviously, the NEP given by this last equation is reduced by the factor $n^{\frac{1}{2}}$ over that of a mechanically scanned single detector. This might well have been obvious since the effective bandwidth has been dras-

-61-

tically reduced since each detector can integrate over a time period which is n times longer than that of a mechanically scanned single detector which can detect the signal from each element in the scene only over a short time period.

The signal to noise ratio can be obtained by taking the ratio of the signal current to Eqn. 7 to the root mean square noise current given by Eqn. 6. In an imaging application, $\Phi = N$, and this yields,

$$S/N = (\eta\ A\ \cdot\ \Phi\ \cdot\ T_I/2)^{\frac{1}{2}}. \tag{10}$$

The maximum signal to noise ratio is limited by saturation of the device due to its limited charge storage capability. If C_o is the gate insulator capacitance and $\Delta\ \psi_s$ the maximum allowed change in surface potential [3] then,

$$\eta\ \Phi\ T_I = C_o\ \Delta\ \psi_s/q = N_S \tag{11}$$

where N_S is the surface charge density at saturation. This gives

$$S/N = (N_S\ A/2)^{\frac{1}{2}}. \tag{12}$$

The maximum signal to noise ratio depends only on the surface charge storage density and the area of the element in the imaging array.

INTEGRATING ACTIVE STATIC CHARGE STORAGE DEVICE, IRFET

The infrared sensing MOSFET, IRFET [6,7,8], will integrate the signal as in the previous case and at the end of this integration period there will be a change in drain to source current, ΔI_{DS}, in the linear region given by:

$$-\Delta I_{DS} = \mu C_o\ (W/L)\ \Delta V_{DS}\Delta V_T T_I\ \sigma N \tag{13}$$

where μ is the effective surface mobility, C_o the oxide capacitance, W/L the width to length ratio of the channel, ΔV_T is the maximum possible change in threshold voltage, σ the photoionization cross section, T_I the integration period, and N the background flux. However, the change in threshold voltage is due to a change of charge in the channel of the device and there will be associated with this, as before in the CID or CCD, some uncertainty in this change in charge due to shot noise.

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As shown in Figure 1, in the infrared sensing MOSFET, the emission of holes from impurity centers in the surface space charge region will induce a change of charge in the channel or inversion layer. This change in charge, ΔQ_{CH} can be written $\Delta Q_{CH} = \bar{I} \, T_I$, where $\bar{I}$ is the average source current. By taking into account the displacement current, or change in width of the surface depletion region [9], it can be shown

$$\bar{I} = q\sigma \, N_{TT} W_d NW \, L/2 \tag{14}$$

and since the quantum efficiency, η, is just

$$\eta = \sigma N_{TT} \, W_d \tag{15}$$

then

$$\bar{I} = q \, \eta \, W \, L \, N/2 \tag{16}$$

Since this is a time dependent process, then by Carson's Theorem there will be a root mean square noise current

$$(I_N^2)^{\frac{1}{2}} = (2 \, q \, \bar{I} \, \Delta\nu)^{\frac{1}{2}} = (q^2 \, \eta \, W \, L \, N/T_I)^{\frac{1}{2}} \tag{17}$$

and a possible error in the charge in the channel at end of this integration period, T_I, of:

$$(Q_N^2)^{\frac{1}{2}} = (q^2 \, \eta \, W \, L \, N/T_I)^{\frac{1}{2}} \, T_I \tag{18}$$

In the linear region of operation,

$$I_{DS} = \mu C_o \, (W/L) \, (V_{GS} - V_T) \, V_{DS} = \mu \, Q_{CH} \, V_{DS}/L^2 \tag{19}$$

$$Q_{CH} = C_o \, (V_{GS} - V_T) \, W \, L \text{ coulombs} \tag{20}$$

A possible error of charge in the channel $(Q_N^2)^{\frac{1}{2}}$ at the end of the integration period will result in a root mean square noise current in the sample period of:

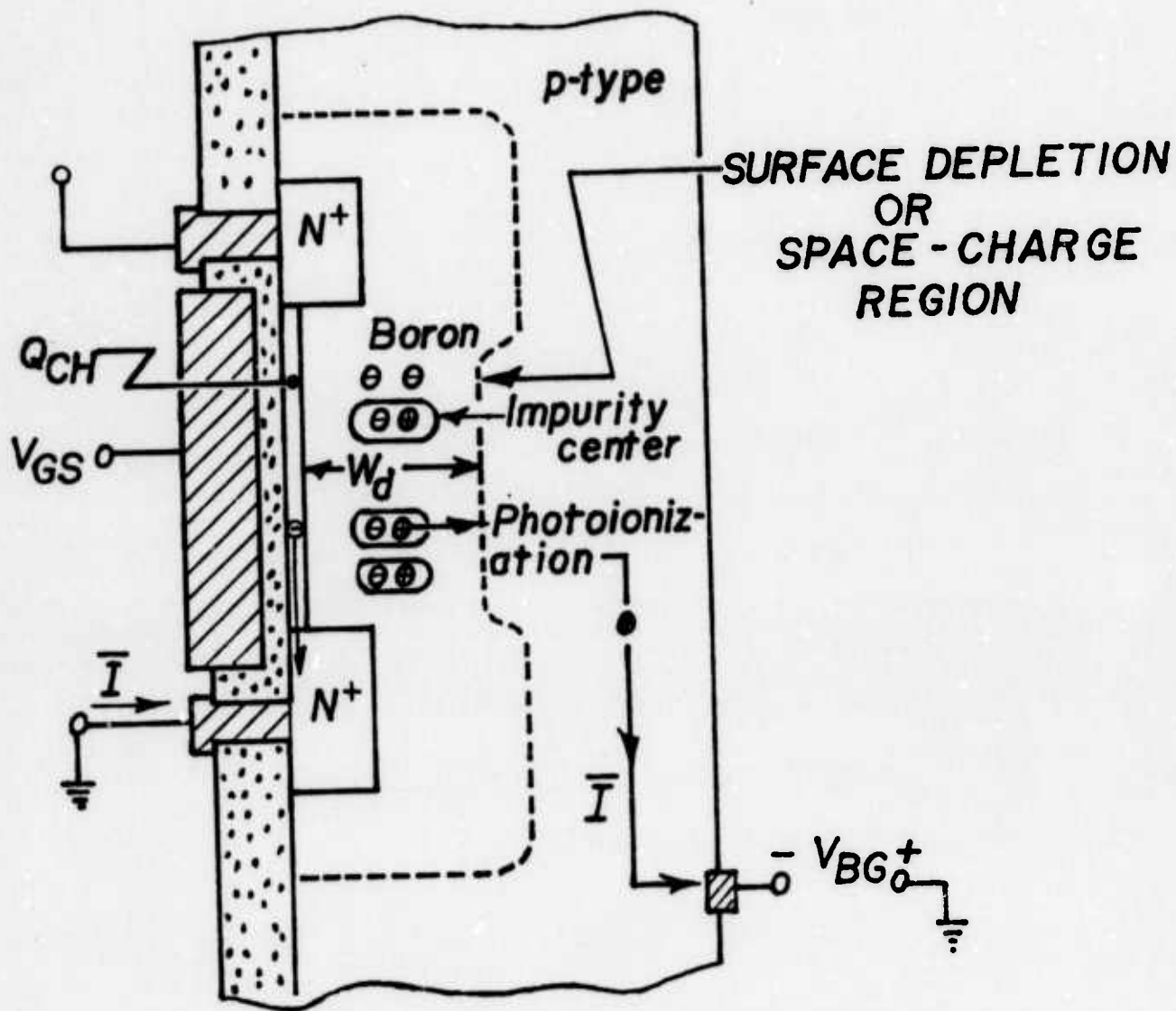$$(I_{DSN}^2)^{\frac{1}{2}} = \mu \, (Q_N^2)^{\frac{1}{2}} \, V_{DS}/L^2 \tag{21}$$

-63-

Figure 1.   The Infrared Sensing MOSFET Showing Source and Substrate
Current, $\bar{I}$, due to Emission of Holes From Impurity Centers

$$= \mu \ (q^2 \ \eta \ W \ L \ N \ T_I)^{\frac{1}{2}} V_{DS}/L^2 \tag{22}$$

The signal current in the sample period will be

$$i_{signal} = \mu \ C_o \ (W/L) \ V_{DS} \ \Delta V_T \ \sigma \phi \ T_I \tag{23}$$

and equating the signal and noise to determine the noise equivalent power yields:

$$\phi = (1/(\sigma C_o \Delta V_T)) \ (q^2 \ \eta \ N/(W \ L \ T_I))^{\frac{1}{2}} \tag{24}$$

However, ΔV_T, can be expressed in terms of the oxide thickness and doping densities [6,8];

$$\Delta V_T = (x_o K_s/K_o) \ (2(2|\emptyset_f| + |V_{BG}|) \ q \ N_A/(K_s e_o))^{\frac{1}{2}}(N_{TT}/2(N_A)) \tag{25}$$

then

$$\Delta V_T = q \ W_d \ N_{TT}/(2C_o) \tag{26}$$

and ϕ becomes

$$\phi = (4 \ N/(W \ L \ \eta \ T_I))^{\frac{1}{2}} \tag{27}$$

and the noise equivalent power, $NEP = \phi \ \hbar w_s \ W \ L$, for a single detector

$$NEP = \hbar w_s \ (4 \ N \ A/(\eta \ T_I))^{\frac{1}{2}} \tag{28}$$

This is just a factor of $(2)^{\frac{1}{2}}$ different than the classical formula for the shot noise limit for background limited operation of a photodiode.

In an imaging application, A the area of each detector can be just $A = A_{IP}/n$, and the integration period T_I can be just the frame time T_F and then $T_I = T_F$. The NEP for a single detector or element in the scene is then:

$$NEP = \hbar w_s \ (4 \ N \ A_{IP}/(n \ \eta \ T_F))^{\frac{1}{2}}. \tag{29}$$

This is a factor of $(n/2)^{\frac{1}{2}}$ smaller than that for a mechanically scanned single detector.

Again the signal to noise ratio can be found by taking the ratio of the signal current in the sample period, Eqn. 23, to the root mean square noise

current in the sample period, Eqn. 22, to give,

$$S/N = (\eta A \, \phi \, T_I/2)^{\frac{1}{2}}. \tag{30}$$

The IRFET will saturate if the product of $\phi \, T_I$ is too large. Saturation will be defined to occur when $T_I = 2 \, \tau = 2/(\phi\sigma) = 2/e_p^o$, and using $\eta = \sigma \, W_d \, N_{TT}$ then the maximum attainable signal to noise ratio is

$$S/N = (W_d \, N_{TT} \, A/2)^{\frac{1}{2}}. \tag{31}$$

The product $W_d \, N_{TT}$ is just the change in charge density in the surface depletion region, if we let

$$N_S = W_d \, N_{TT} \tag{32}$$

then

$$S/N = (N_S \, A/2)^{\frac{1}{2}}. \tag{33}$$

Eqn. 33 has exactly the same form as Eqn. 12 since N_S is a surface charge density and A is the area of an individual element.

CONCLUSIONS

It has been shown that the theoretical background limited (BLIP) noise equivalent power for an array of n-detectors, CCD, CID, or IRFET is reduced by a factor of $n^{\frac{1}{2}}$ from that of a mechanically scanned single detector. Furthermore, all surface type devices CCD, CID, or IRFET have the same maximum attainable signal to noise ratio, $S/N = (N_S \, A/2)^{\frac{1}{2}}$. The maximum attainable signal to noise ratio depends only on the stored surface charge density, which is comparable in all surface devices, and the area of the device. It is independent of the quantum efficiency, η, integration period, T_I, and all other considerations.

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NOISE MEASUREMENTS ON INFRARED SENSING MOSFET's

Measurements on shot and 1/f-type noise mechanisms in an infrared-sensing MOSFET (IRFET) are reported. The results are interpretable from a physical understanding of the device operation.

INTRODUCTION

If a cooled gold-doped IRFET [1] is preset by turning it off and accumulating the surface, then the gold impurity centers are ionized by the capture of holes (positive charge state) and remain filled in the surface depletion region which results when positive gate voltage is applied. The conductance of the IRFET channel is a function of the number of ionized impurity centers in the depletion layer through the space-charge dependence of threshold voltage. As infrared radiation, i.e., 1.77 to 3.54 μm, now illuminates the device, the gold centers (donor level) in the surface space-charge region discharge by emitting holes to the silicon valence band. The IRFET thus integrates the incident photon flux, and at the end of some integration period the drain-to source current in the saturation region will have decreased by an amount

$$\Delta I_{DS} = - \frac{\mu \, WQ_{CH}}{L \, C_o} \, \Delta Q_{CH \, max} \, [1 - \exp(-t_I/\tau_D)] \qquad (1)$$

where ΔI_{DS} is the change in drain current, μ is the effective surface electron mobility, W/L is the geometric width-to-length ratio of the

channel, Q_{CH} is the charge per unit area in the channel before illumination, C_o is the oxide capacitance per unit area, $\Delta Q_{CH\,max}$ is the maximum change in channel-charge per unit area, t_I is the integration time, and τ_D is the time constant associated with emission of holes from the gold donor level. The device is analog and the dynamic range is limited only by the condition that t_I must be less than or equal to 2.3026 τ_D. τ_D is defined as the reciprocal of the product $\Phi \sigma_{p-1}^o$, where Φ is the incident photon flux ($\#/cm^2 \cdot sec$) and σ_{p-1}^o is the photoionization cross section (cm^2) of holes trapped at the gold donor level. However, the minimum detectable photon flux is restricted by the noise arising from various sources intrinsic to the device, i.e. thermal noise of the conducting channel, shot noise and interface-state noise (i/f-type). Since the IRFET is a static, integrating detector whose output is a difference signal, extrinsic noise sources, i.e., electrical input noise and bias/reset noise, can be assumed negligible as performance-limiting considerations. It has been predicted that infrared-sensing MOSFET's are inherently low-noise devices and that the noise introduced does not limit applications of IRFET's in image sensing[1]. A series of noise measurements have been conducted in order to evaluate the relative magnitudes of the various noise sources in practical devices. Noise theory for the background-limited operation of an array of IRFET's has been recently developed [2]. In this paper are presented the results of careful noise measurements in a gold-doped, n-channel, infrared-sensing MOSFET.

EXPERIMENTAL APPARATUS

The device used in these measurements was made on a (100) orientation, p-type substrate of 1-2 $\Omega \cdot cm$ resistivity and doped with a gold concentration of 2×10^{15} cm^{-3}. The gate oxide of the MOSFET is 4000 $\overset{o}{A}$ thick, and the

circular channel has an 8.17 W/L ratio providing an active area of
2.5×10^{-3} cm^2. By mounting the device on a TO-5 header fitted in a
tubular reflective cavity, both frontside and edge illumination was
possible.

The experimental arrangement and the equipment used in these
measurements are shown in Fig. 1. The upper-corner frequency of the
Hewlett-Packard DC Micro Volt-Ammeter 425A is 1-Hz (-3db), and the
lower-corner frequency of the Krohn-Hite 3750 Filter (high pass) is
adjustable from 0.02-Hz; therefore, the two instruments provided for a
variable noise bandwidth. A Bausch and Lomb tungsten light source
powered from a variac permitted various photon flux intensities. The out-
put signal current and the accompanying noise was measured with the IRFET
running continuously and recorded by a Houston Instrument Omnigraphic
2000 X-Y Recorder. A 1-µF DC-blocking capacitor was attached to the input
of the X-Y recorder (1-MΩ input impedance) in order to eliminate any drift
in the high-pass filter/volt meter output. This circuit attenuated all
frequencies below 0.159-Hz, thus limiting the magnitude of the 1/f type noise.
The incident photon flux was determined by noting the time t_F required for
$|\Delta I_{DS}|$ to increase from 0.1 to 0.9 of its final value (cf. Fig. 2).

EXPERIMENTAL RESULTS

The overall system noise with the high-pass filter input shorted was about
8mV$_{rms}$ at the volt meter output. The IRFET was connected in a common
source configuration with a precision 1 kΩ load resistor.

A. Interface-State Noise

The flow of electrons from one site to another in the surface channel
of a MOSFET is a random process because of trapping and emission of carriers
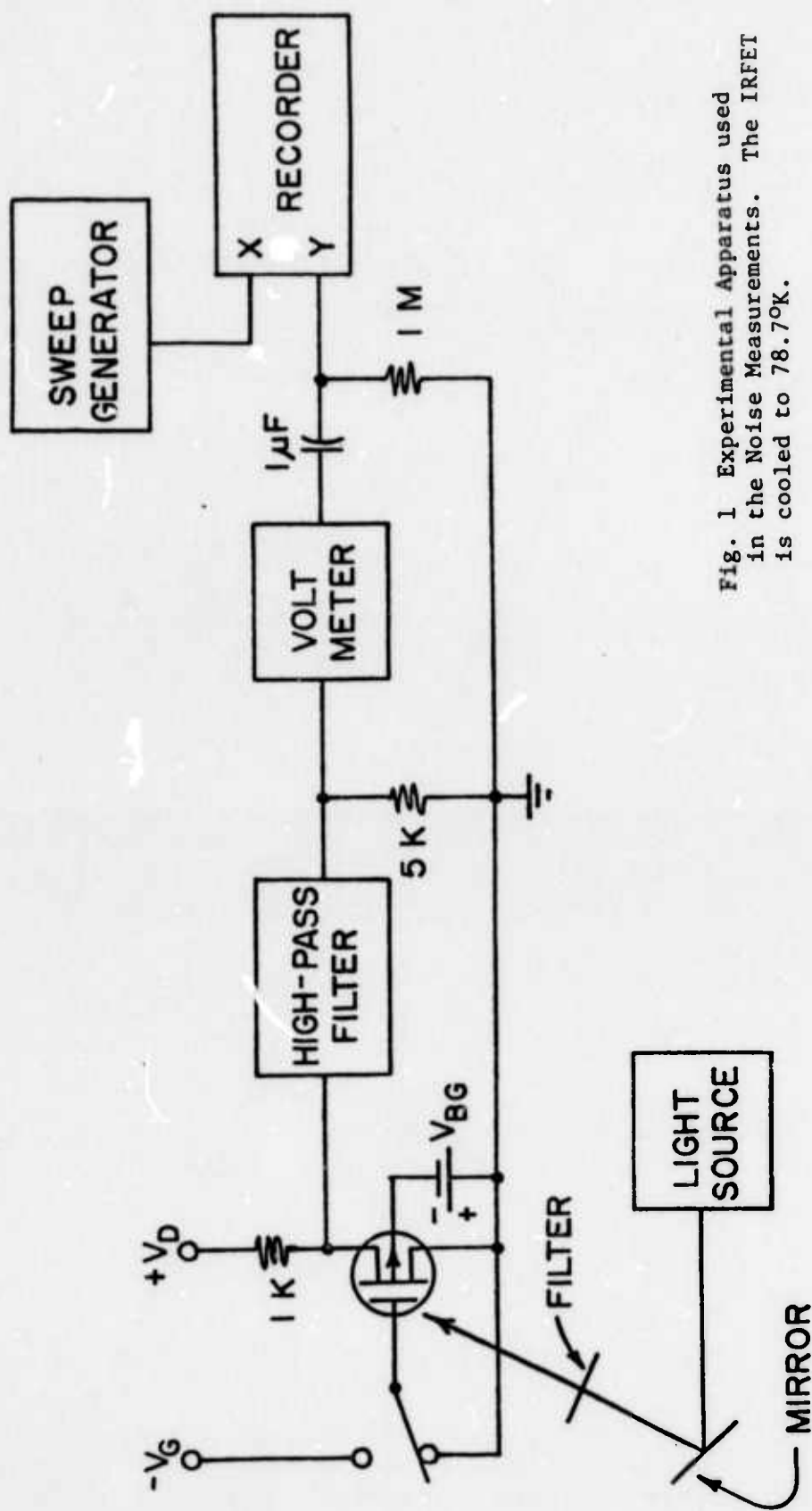
Fig. 1 Experimental Apparatus used
in the Noise Measurements. The IRFET
is cooled to 78.7°K.

Fig. 2 Time Required for Gold Centers to Discharge as a Function of Incident Photon Flux.

$$t_F = 1.4648 \times 10^{16}/\Phi$$

DISCHARGE TIME, SEC →

PHOTON FLUX, NUMBER PER CM^2 PER SEC →
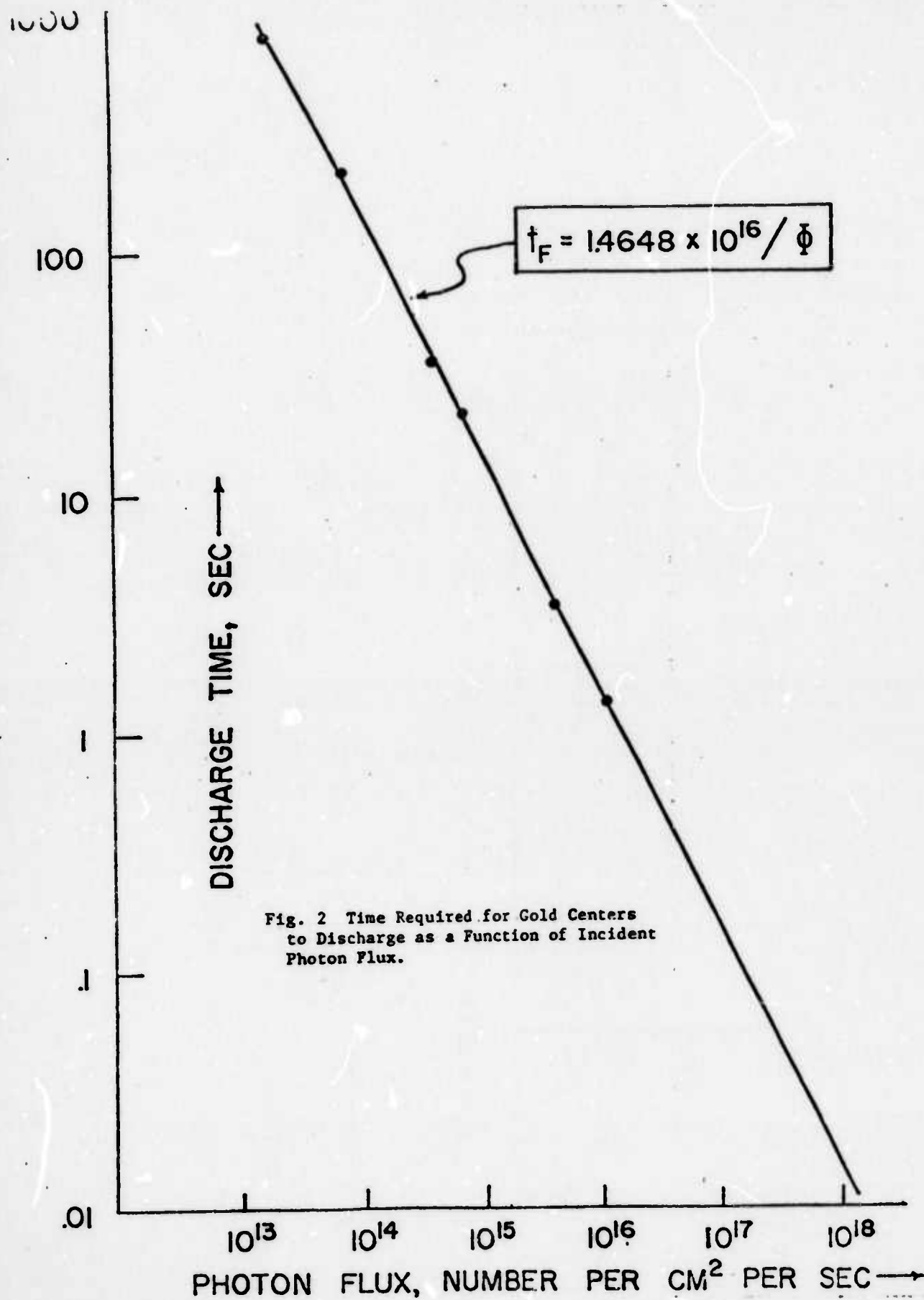
by interface states [3]. Slow interface states (oxide states) produce noise in IRFET's during integration. Whenever the device is active, both fast and slow interface-state noises are present as a dark current with 1/f-type dependence [4].

This dark-current noise was observed in different bandwidths for 170 sec by varying the lower corner frequency of the high-pass filter from 0.16 to 4-Hz (10db gain after 1-Hz) and recording the RMS noise voltage across the 1 kΩ load resistor versus time. By taking the difference in noise current between two observations differing by $\Delta f = 0.2$ Hz and dividing by 0.2 Hz, the dark-current noise was specified for a given center frequency in a 0.2-Hz bandwidth. The results of this series of measurements are shown in Fig. 3 (note that $1/f = t_I$). Fitting the experimental points to a straight line (method of least squares) indicates that the dark-current noise in a cooled IRFET varies approximately as $(1/f)^{1.8}$.

B. Shot Noise

By illuminating the IRFET with infrared light, the shot (or quantum) noise associated with the optically generated change in the channel-charge could be measured. According to theory [2], this change in charge, ΔQ_{CH}, can be written as

$$\Delta Q_{CH}(t) = \bar{I}_S \, t_I, \tag{2}$$

where $\bar{I}_S$ is the average source current per unit area. Due to the random arrival of the photons, the mean-square noise current is

$$i_{n,rms} = \sqrt{2 \, q \, \bar{I}_S \, A \, \Delta \nu} \tag{3}$$

where $A(=WL)$ is the active area of the device and $\Delta\nu$ is the bandwidth. By combining Eqs. (1) and (2) and solving the resulting expression for $\bar{I}_S$, Eq. (3) may be rewritten as

$$i_{n,rms} = \sqrt{\frac{2 \, q \, \Delta I_{DS \, max} \, [1 - \exp(-t_I/\tau_D)] \, L \, C_o \, A \, \Delta \nu}{\mu W \, Q_{CH} \, t_I}} \tag{4}$$
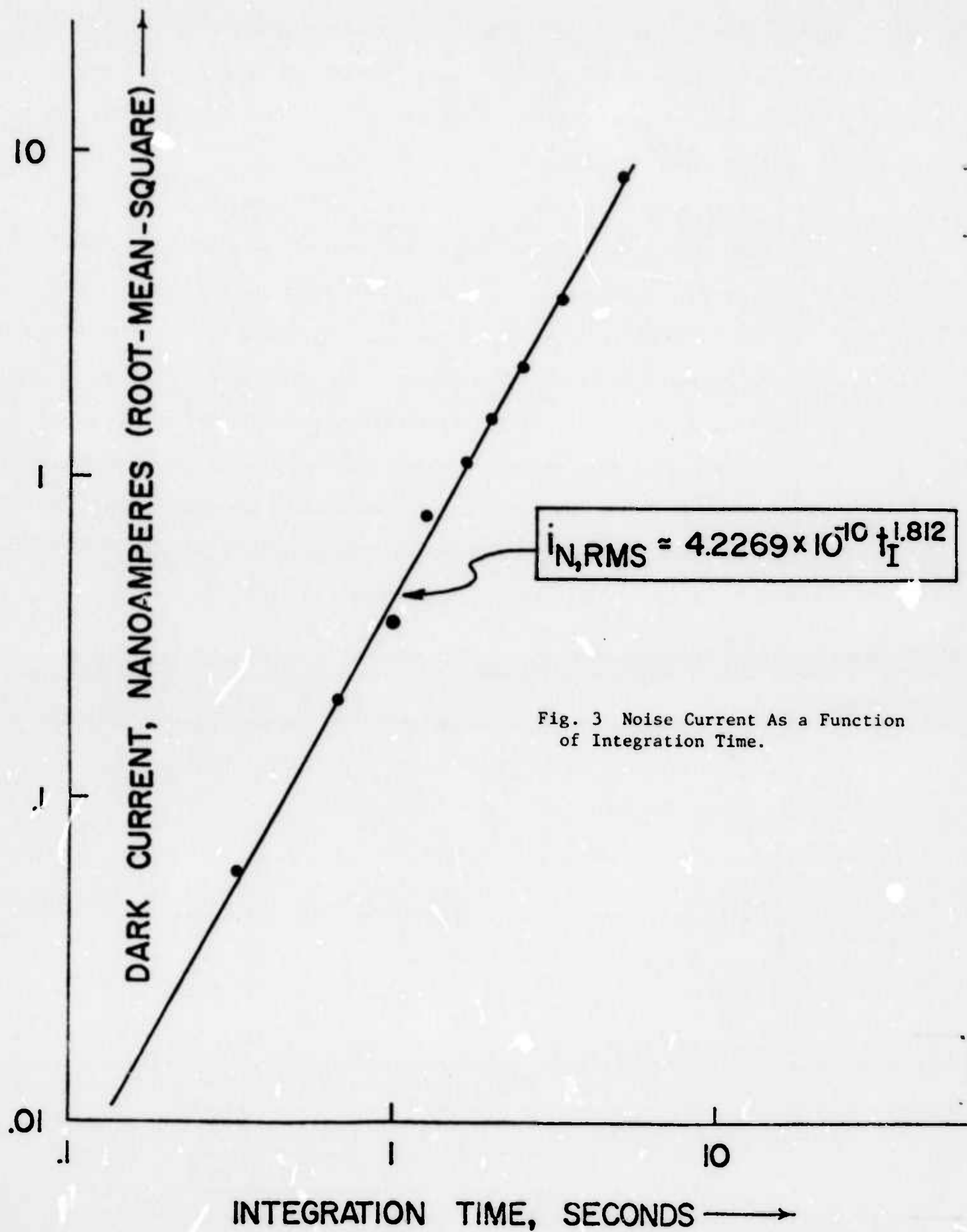
Fig. 3 Noise Current As a Function
of Integration Time.

$$i_{N,RMS} \cong 4.2269 \times 10^{-10} \, t_I^{1.812}$$

DARK CURRENT, NANOAMPERES (ROOT-MEAN-SQUARE) ⟶

INTEGRATION TIME, SECONDS ⟶

or the mean-square fluctuation in the channel-charge per unit area at the end of the integration period is

$$Q_{N,rms} = \frac{i_{n,rms}\, t_I}{A} = \sqrt{\frac{2\, q\, \Delta I_{DS\ max}\, [1 - \exp(-t_I/\tau_D)]L\, C_o\, \Delta\nu\, t_I}{\mu\, W\, Q_{CH}\, A}} \qquad (5)$$

where $\Delta I_{DS\ max}$ is the maximum drain-to-source photocurrent. This possible error in channel-charge per unit area, $Q_{N,rms}$, will cause a mean-square noise current $i_{DS\ n,rms}$ at the output of

$$i_{DSn,\ rms} = \frac{\mu\, W\, Q_{CH}}{L\, C_o}\, Q_{N,rms} \qquad (6)$$

during integration. Eq. (6) should be interpreted as an upper-bound limit since the average source current due to the optical emission of holes from the gold impurity centers in the surface depletion region is inversely proportional to the integration time ($t_I \geq 0.1\, \tau_D$).

A typical result comparing the measured dark-noise and shot-noise currents in a bandwidth $\Delta\nu = 0.2$-Hz is shown in Fig. 4. During illumination the noise current is seen to eventually approach the dark noise level as the length of the integration period increases. In order to observe the initial shot-noise current immediately after the IRFET was illuminated, the time scale was expanded (see Fig. 5). A good agreement between the measured shot noise ($i_{n,rms} \simeq 0.5\, i_{n,p-p}$) and the theoretical values to within 16-percent error is observed.

The expected drain-to-source noise current for two different integration times is plotted as a function of incident photon flux in Fig. 6. Note that the input circuit of the X-Y recorder limits 1/f-type

VERTICAL SCALE: 100 NANOAMPS/INCH

HORIZONAL SCALE: 50 SECONDS/INCH

$\frac{1}{f}$ NOISE = 40 NANOAMPS, P-P

$\frac{1}{f}$ NOISE + SHOT NOISE $\Big|_{t=50}^{t=10}$ = 60 NANOAMPS, P-P

$\bar{\phi} \approx 6.67 \times 10^{13}$ PHOTONS/CM^2·SEC

t=0

CIRCUIT NOISE
IRFET
(DURING ILLUMINATION)

CIRCUIT NOISE
IRFET
(DARK)

INFRARED
SOURCE
AGAIN ON
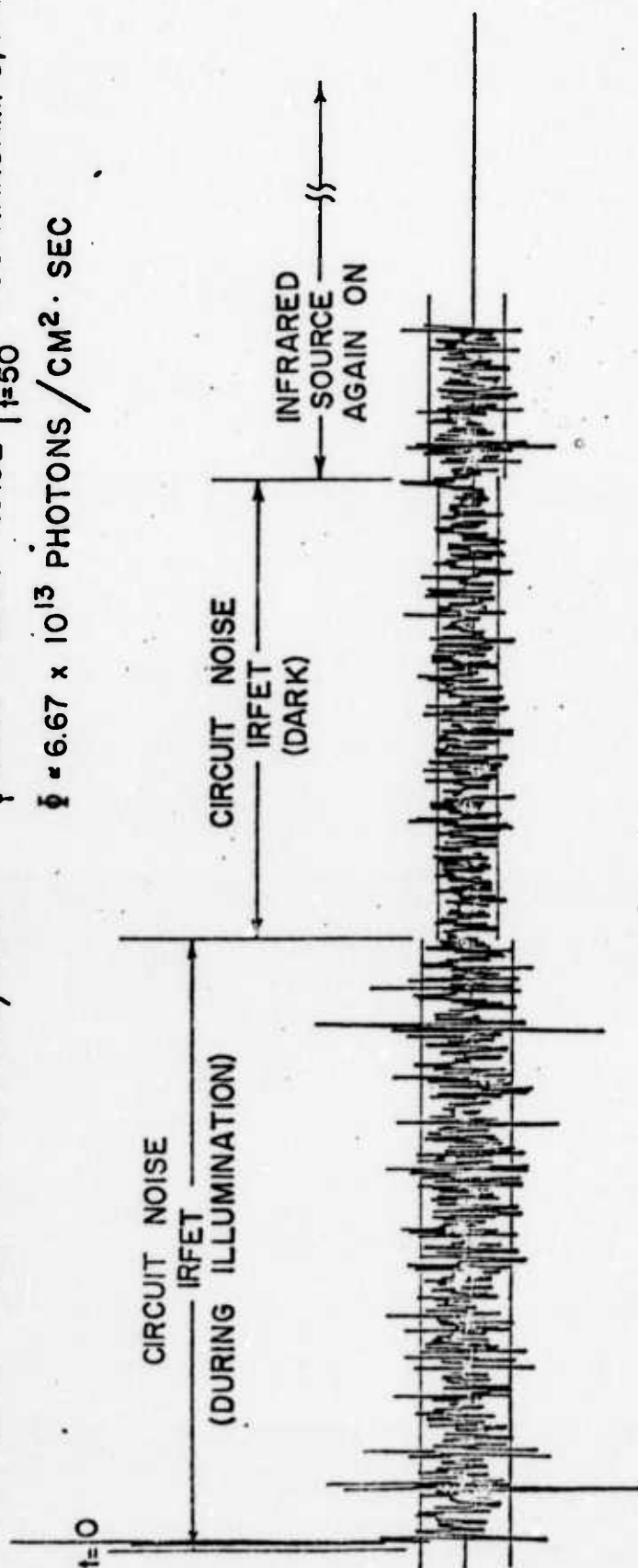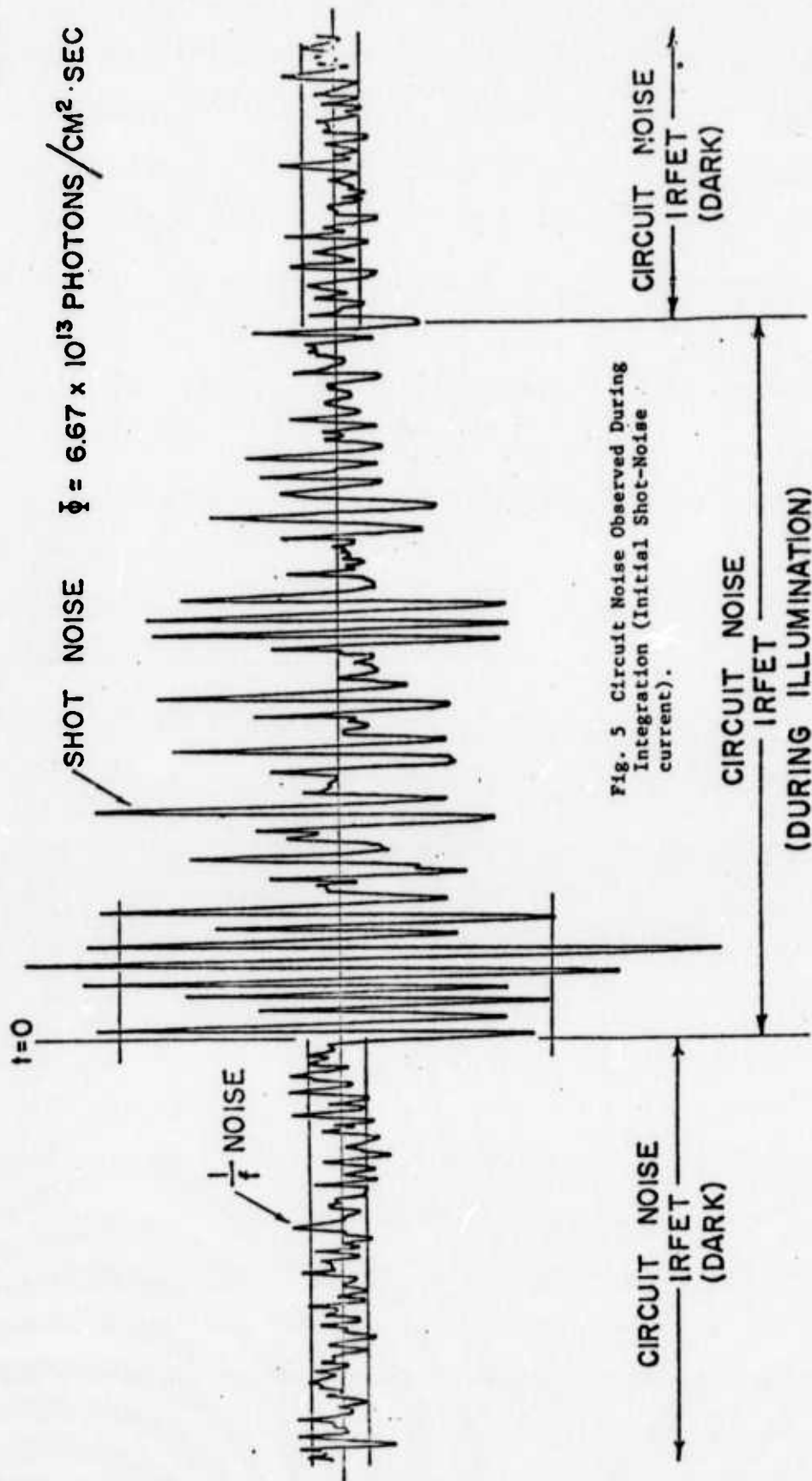
Fig. 4 Circuit Noise Observed During Illumination and Dark (Source Off).

VERTICAL SCALE: 100 NANOAMPS/INCH

HORIZONAL SCALE: 10 SECONDS/INCH

$\frac{1}{f}$ NOISE = 40 NANOAMPS, P-P

$\frac{1}{f}$ NOISE + SHOT NOISE $\Big|_{t=0}^{t=0}\Big|_{t=10}$ =300 NANOAMPS, P-P

$\Phi = 6.67 \times 10^{13}$ PHOTONS/CM^2·SEC

Fig. 5 Circuit Noise Observed During Integration (Initial Shot-Noise current).

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circuit noise to approximately 12 mA,RMS (cutoff frequency $f_C = 0.159$-Hz, or $t_I = 6.3$ sec); thus, shot noise could still be observed for long integration periods. The observed noise current for $t_I = 100$ sec is shown as a dotted line. However, the expected actual noise (1/f-type dominant) as would be seen by a static-change (DC) meter is much larger, and is shown as a solid line. Also, when $t_I > 2.3026 \, \tau_D$, the dynamic range of the IRFET is saturated and the device can no longer register any incident infrared radiation. In this forbidden range of operation, the shot noise reaches a momentary maximum value, which is constant for $t_I \, \Phi \, \sigma_{p-1}^o \geq 2.3026$ while all the gold centers discharge, and afterwards goes to zero; therefore, only dark-noise current will be present in the IRFET after time $t = 2.3026 \, \tau_D$.

The shot-noise limited portions of both curves in Fig. 6 were calculated by regarding the product $\overline{I}_S t_I$ as the average change in channel-charge, i.e., $\overline{\Delta Q_{CH}} = \overline{I}_S t_I = \Delta Q_{CH}(t)/2$, or $i_{DS \, N,P-P} \simeq 2\sqrt{2}$ times the expected RMS noise current from the graph. For an incident photon flux $\Phi = 6.67 \times 10^{13} \mathrm{cm}^{-2} \mathrm{sec}^{-1}$, the theoretical drain-to-source noise current is $348 \, \mathrm{n A}$, P-P as compared to the measured value of $300 \, \mathrm{nA}$, P-P in Fig. 5.

Fig. 6 has been divided into three distinctly different regions which are representative of the different operating conditins. In the saturated region the photon flux is too large and the integration period too short to allow operation of the device as a photon detector, all the impurity centers discharge before the end of the integration period. In the 1/f noise limited region, which corresponds to low photon fluxes and long integration periods, 1/f rather than shot noise is the limiting factor. In the shot noise or background limited region, which corresponds to relatively speaking higher photon fluxes and shorter integration periods, shot noise due to the incident photon flux is the dominant noise mechanism. It is shown that shot noise or background limited operation of the IRFET can be acheived for integration periods of less than about ten seconds or with photon fluxes above about $10^{15} \, \mathrm{cm}^{-2} \, \mathrm{sec}^{-1}$.

Fig. 6 Output Noise Current as a Function of Incident Photon Flux and Integration Time
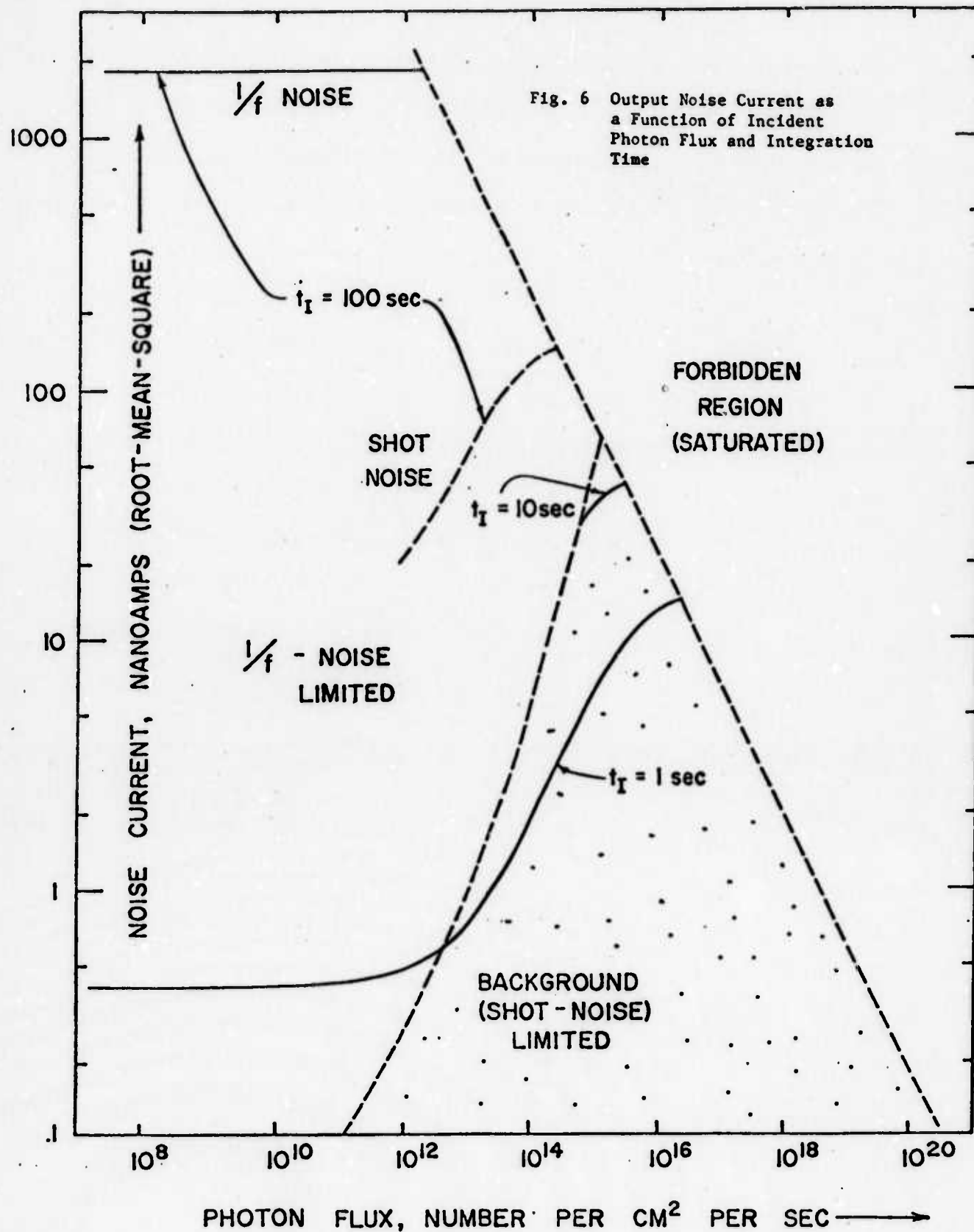
DISCUSSION AND CONCLUSIONS

The thermal noise of the conducting channel in an IRFET can be neglected (except for very short integration times and small photon fluxes) since the device is operated at low temperatures [5,6]. In view of the results of the noise measurements above, it seems that the dominant noise mechanism for long integration periods and low photon fluxes in an IRFET is 1/f. Shot noise becomes a limiting consideration only for short integration periods and high photon fluxes.

In conclusion, these measurements indicate that the noise levels due to shot and interface-state noise sources agree with a physical understanding of the IRFET's operation. Careful design of output-sensing instrumentation and optimization of integration time/photon flux factors should enable the broad application of infrared-sensing MOSFET's in imaging schemes where background(shot-noise) limited operation is desirable.

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CONCLUSIONS

Operation of the gold-doped infrared sensing MOSFET(IRFET) has been demonstrated and treated in detail in previous documents.

Experimental verification has been provided of operation of the indium doped infrared sensing MOSFET and the optical reponse and device characteristics examined. The results correspond to those anticipated on the basis of prevously available information and a design analysis. More work remains to be done in extending the optical measurements out to longer wavelengths and also perhaps in obtaining wafers with a more optimum doping ratio between the indium and boron concentrations. Work is anticipated to continue on these aspects for another three to four months.

Double doped, gallium and boron doped,wafers have been produced by the diffusion of gallium from a doped oxide source into a boron doped wafer. MOSFET devices have been fabricated and preliminary results obtained on the operation of the gallium doped silicon infrared sensing MOSFET. These devices also appear to work according to the original design proposal and criteria. This work is just getting underway.

Noise measurements indicate that shot noise or background limited operation can be acheived for integration periods of about less than 10 seconds.

While the results are by no measure complete, on the other hand all results obtained up to this point in the work indicate that indeed the IRFET can operate in the near, middle, and far infrared wavelength regions and under shot noise or background limited conditions. These aspects combined with the unique features of the IRFET are anticipated to make it usefull in infrared imaging arrays.